Design Feature

A. ATTARAN | Engineer
Center of Research and Applied Electronics (CRAE), University of Malaya, 50603, Kuala Lumpur, Malaysia; 006-0379675248, FAX: 006-0379675316, e-mail: Aliyar.attaran@gmail.com.

M. MOGHAVVEMI | Engineer
Center of Research and Applied Electronics (CRAE), University of Malaya, 50603, Kuala Lumpur, Malaysia, 006-0379675248, FAX: 006-0379675316, e-mail: Mahmoud@um.edu.my and College of Electrical Engineering, University of Tehran, Tehran, Iran.

H. AMERI | Professor
Center of Research and Applied Electronics (CRAE), University of Malaya, 50603, Kuala Lumpur, Malaysia, 006-0379675248, FAX: 006-0379675316, e-mail: Itmwave@streamyx.com.

Fabricate a 2.4-GHz Fractional-N Synthesizer

Fractional-N frequency synthesizers offer numerous advantages in terms of performance compared to integer-N frequency synthesizers for emerging wireless communications applications.

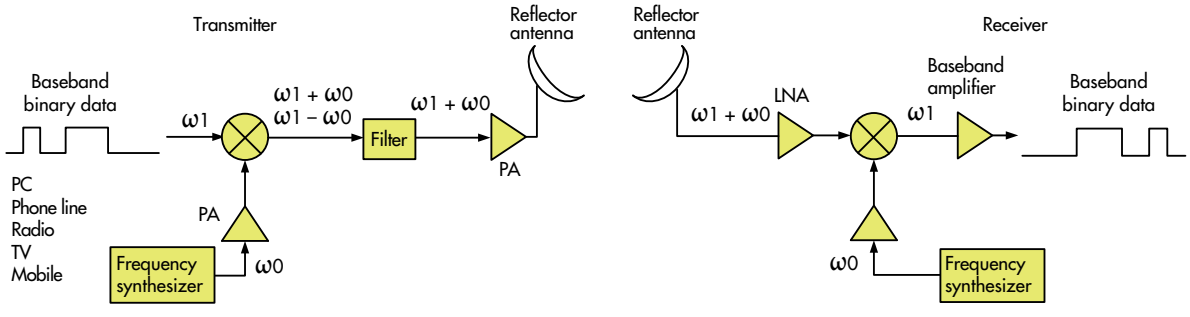
Frequency synthesizers are used throughout communications systems for tuning the signal frequencies needed for receiving and transmitting. As silicon CMOS technology has been applied at higher frequencies, it has helped the expansion of wireless technology to a wide range of applications.[1,2] These synthesizers have supported applications requiring tuning with fine resolution—from kHz steps to a few MHz—and low phase noise, on the order of –100 dBc/Hz offset 10 kHz from the carrier.

Many of these synthesizers have been developed as integrated-circuit (IC) solutions.[3] In terms of circuit architectures, integer-N frequency synthesizers are often challenged in meeting performance requirements such as loop bandwidth, phase noise, and channel spacing due to the fundamental design of the integer-N divider modulus.

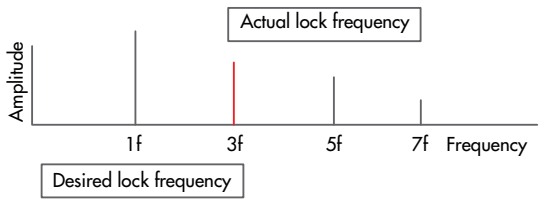
In contrast, a fractional-N frequency synthesizer can provide the loop bandwidths needed for many of these emerging wireless applications, with fine channel spacing. In addition, they can achieve low phase noise without excessive reference spurious levels. Since a fractional-N frequency synthesizer uses a higher phase/frequency-detector (PFD) comparison frequency and lower division ratio than an integer-N frequency synthesizer, low-frequency phase noise can be suppressed to a high degree in a fractional-N synthesizer.[5]

Figure 1 represents a typical RF wireless transceiver system, showing the role of the frequency synthesizer in both transmitter and receiver sections.[6] Essentially, the frequency synthesizer must cover a required frequency range with adequate output power—as well as acceptable levels of signal integrity and signal purity—with the capability of tuning to meet channel spacing requirements.[7] Locking or stabilizing the frequency synthesizer usually works around a specific frequency but, depending upon adjacent components, a synthesizer's locking loop may favor other frequencies.[8]

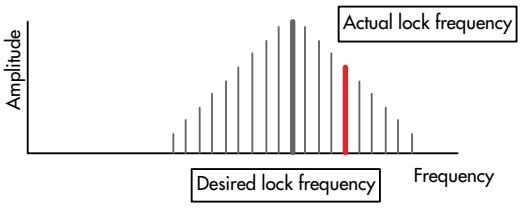
For example, harmonic locking can occur when harmonic frequencies have sufficient amplitude levels to engage the



1. This simple block diagram shows the main components of a basic communications transceiver.



2. This simple plot depicts locking at a third-harmonic frequency.



3. This plot depicts locking at an adjacent frequency.

synthesizer's locking loop. This type of locking usually occurs with square waveform modulation where multiples of the desired frequency have sufficient power to cause locking. Long runs of zeros in data bit causes phase detector favors fractional and non-fractional harmonics.[9] Side-locking occurs when periodic modulation produces discrete spectral lines with enough energy to cause a synthesizer's loop to lock to one of these spectral lines.

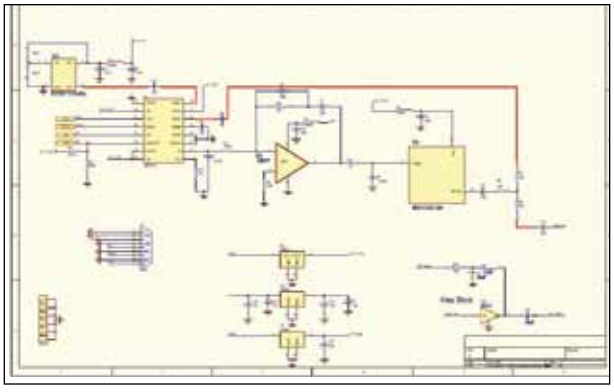
The primary spurious frequencies generated in integer-N frequency synthesizers come from reference spurious signal products. The step size and loop bandwidth relationship dictate the spurious attenuation level that can be tolerated for a given synthesizer design. In contrast, spurious signal products in a fractional-N structure emanate from the fractional modulus. Fractional spurious signals appear around the voltage-controlled-oscillator (VCO) carrier frequency regardless of which frequency it is programmed to. The spacing between the first three spurious products is usually equal to the step size or one-half of the channel step size. In a fractional-N frequency synthesizer, the comparison frequency or step size is typically high, which leads to large loop-filter attenuation of the reference spur (even with a wide loop bandwidth implementation).

TABLE 1: SIMULATING PHASE NOISE AT 2.8 GHz

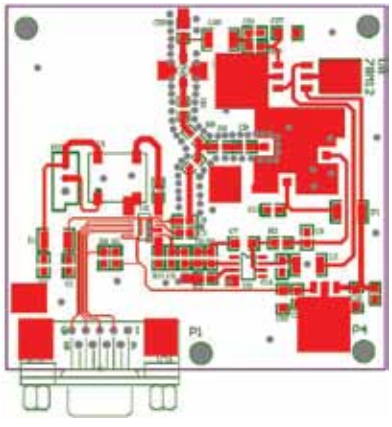
Offset frequency	Phase noise (dBc/Hz)				
	ADF4118	ROS-2432-119+	TXO10	OP27	Total
100 Hz	–69.33	–42.70	–90.37	–51.87	–42.44
1 kHz	–107.9	–72.88	–148.8	–76.14	–72.68
10 kHz	–164.8	–100.00	–218.9	–99.85	–96.92
100 kHz	–224.8	–123.0	–279.7	–119.9	–118.2
1.00 MHz	–284.6	–143.0	–300.0	–139.9	–138.2

Boundary spurious products appear in an integer-N structure when the synthesizer's VCO is programmed to frequencies near harmonic multiples of the comparison frequency. But all fractional-N synthesizers also exhibit these spurious products. These spurious signals are at lower amplitude levels than primary integer-N spurious products located at a harmonic of the comparison frequency. Whether or not these spurious products represent problems in a synthesizer design depends on the loop bandwidth, the comparison frequency, the system spurious specification, and the required frequency band plan.

In a performance comparison, a fractional-N structure provides better step resolution and a faster locking process



4. This pre-layout schematic diagram was created with the help of Protel design software.



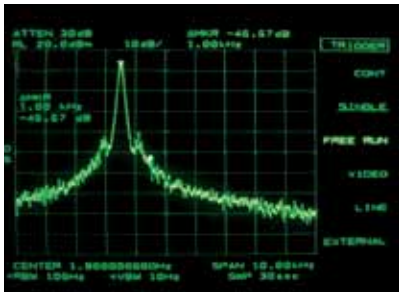
5. This layout represents the 1.8-to-2.4-GHz frequency synthesizer.

than an integer-N structure. With the latter, widening the loop bandwidth in order to increase the locking process and step size can cause reference spurious frequencies to emerge. In an integer-N synthesizer, the VCO divider (divider N modulus) integer is also large due to the low comparison frequency, resulting in poor phase-noise performance compared to a fractional-N synthesizer.

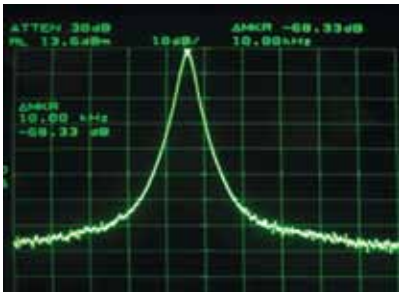
The primary spurious frequencies in this design are from reference spurious signals. The synthesizer step size and loop bandwidth relationship dictates the attenuation level of these spurious products. The spacing between the first three spurious products is usually equal to the step size or one-half the channel step size. For optimum reduction of spurious levels, a step size of 200 kHz and loop bandwidth of 100 Hz were established for the fractional-N frequency-synthesizer design. Widening the loop bandwidth would increase the locking speed and step size, but would also increase the number and levels of spurious products.

After validating the results from computer simulations *(Fig. 4, Table 1)*, a printed-circuit-board (PCB) layout of the fractional-N frequency synthesizer was created with the help of Protel software *(Fig. 5)*. This PCB design/layout software, which was originally developed by Altium (www.altium.com; formerly Protel), is available for free download from a number of different websites. Altium also offers higher-level software tools, including Altium Design. The synthesizer was fabricated as a PCB *(Fig. 6)* and evaluated at center frequencies of 1.8 and 2.1 GHz

6. This photograph shows the fabricated 1.8-to-2.4-GHz frequency synthesizer.



7. This screen shows a spectrum view of the synthesizer at 1.80 GHz.



8. This screen shows a spectrum view of the synthesizer at 2.10 GHz.

(Figs. 7 and 8) with the help of a model HP8563A spectrum analyzer from Agilent Technologies (www.agilent.com).

Spurious performance is less impressive at 2.1 GHz than at 1.8 GHz. The bandwidth for the 1.8-GHz measurements was narrower, so that the phase noise will be superior at the lower band frequencies. The spectrum analyzer's span was set to 50 kHz, with a resolution-bandwidth (RBW) filter at 1 kHz and a video-bandwidth (VBW) filter set at 10 Hz. The 55.67-dB power difference between the carrier and the phase noise, offset 10 kHz from the carrier, indicates that the phase noise level will be:

Phase noise (at 2.1 GHz) = −68.33 − 10log(RBW) = −98.33 dBc/Hz.

The fractional-N frequency synthesizer was evaluated for phase noise at carrier frequencies from 1.8 to 2.4 GHz at 100-MHz intervals and for offset frequencies of 1 kHz, 10 kHz, 100 kHz, and 1 MHz. The results are compiled in *Table 2*. The synthesizer achieved respectable phase-noise performance, with a level of −98 dBc/Hz offset 10 kHz from the carrier. MW

TABLE 2: PHASE NOISE MEASUREMENTS AT VARIOUS OFFSETS FROM 1.80 THROUGH 2.46 GHz.

Carrier frequency (GHz)	Offset at 1 kHz (dBc/Hz)	Offset at 10 kHz (dBc/Hz)	Offset at 100 kHz (dBc/Hz)	Offset at 1 kHz (dBc/Hz)
1.8	−70.3	−96.17	−113.0	−124.5
1.9	−68.8	−97.3	−111.5	−124.5
2.0	−72.0	−97.0	−112.0	−125.0
2.1	−68.5	−98.0	−113.0	−125.0
2.2	−70.0	−98.3	−115.0	−125.0
2.3	−67.5	−98.6	−114.0	−124.0
2.4	−68.0	−99.0	−115.0	−131.0
2.46	−68.5	−99.0	−114.0	−125.0

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