Design Feature

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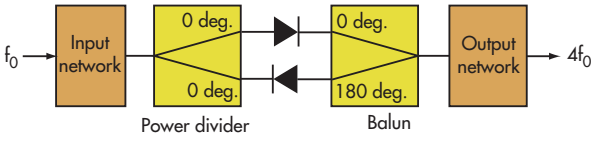
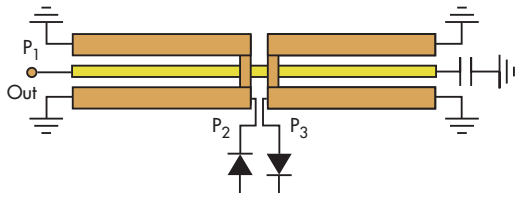
Quadrupler Cuts Losses At W-Band

A unique design approach aids in the fabrication of a W-band quadrupler with low conversion loss that is capable of as much as +2 dBm output power from 80 to 100 GHz.



1. The block diagram depicts the balanced quadrupler.



2. This diagram shows the simple design of the CSDBQ structure.

Schottky diode quadruplers provide practical means of generating signals at higher frequencies, especially when they can perform such functions with minimal conversion loss (CL). Lower loss generally means higher power levels at the output of the quadrupler and, fortunately, with the aid of a commercial computer-aided-engineering (CAE) software program, it has been possible to design a Schottky diode multiplier with low CL for applications requiring signals from 80 to 100 GHz. This monolithic frequency multiplier was fabricated with a 0.1-µm GaAs pseudomorphic-high-electron-mobility-transistor (pHEMT) process and provides as much as +2 dBm output power across its 20-GHz output bandwidth.

Due to their nonlinear characteristics, Schottky diodes are often the key elements in passive frequency multipliers. They are capable of producing stable, low-noise multiplied output signals when combined with an appropriate oscillator.[1] Unfortunately, as the frequency increases, the dielectric circuit losses and roughness of the conductor surface can result in increases in the CL of a Schottky diode multiplier. As a result, one of the design goals when working with these components involves minimizing the CL.

A number of researchers have explored different approaches to passive multiplier designs,[2-4] with the importance of impedance matching for the source and load impedances of the Schottky diodes detailed in ref. 2, although an impedance-matching method or solution was not provided. A W-band frequency doubler was presented in ref. 3, with a quarter-wavelength short stub (at the fundamental frequency) used to provide a short circuit for the second-harmonic frequency at the input of the diode, and a quarter-wavelength open stub (at the fundamental frequency) used to short the fundamental frequency at the output of the diode.

This study did not present the effects of these stubs on CL performance, however. A similar design approach was presented in ref. 4.

Work in ref. 5 detailed a method for optimizing the input and output impedances to a high-gain active frequency multiplier with reflector networks. A similar approach was used in ref. 6 to optimize a frequency tripler. A W-band active frequency doubler was designed and fabricated with a 0.15-µm InGaAs/InAlAs/GaAs mHEMT process in ref. 7. These reports offered several different approaches for designing high-frequency multipliers, but with little description of CL optimization methods for the passive balanced multipliers. The present report examines the importance of impedance matching for the input and output multiplier ports, using input and output reflector networks to not only impedance-match to the impedances of the diodes, but to reduce the CL of the balanced multiplier.

One method of reducing the CL of a diode multiplier is to focus on the Schottky diode and its supporting circuitry. This can be done by examining the construction of a Schottky diode quadrupler, the design of the component's balun, opti-

mization of the input power network and the input/output reflector networks, optimization of the full quadrupler, and fabricating and testing the quadrupler to check how the modeled results compare with actual performance.

Figure 1 offers a block diagram of a generic balanced multiplier, with an antiparallel diode-pair structure used with a balanced-mixer configuration.[8] In this configuration, only even-harmonic frequencies are available at the output, with inherent rejection fundamental-frequency and odd-harmonic signals at the output.

As Eq. 1 shows, the nonlinear Schottky diode current-voltage (I-V) curves are closely related to the input signal amplitude. The input power can be optimized to obtain minimum CL from the multiplier by analysis of Eq. 1:

$$I = I_0[\exp(V_A/V_T) - 1] \quad (1)$$

where:

I_0 = the reverse saturation current;
V_A = the diode external voltage; and
V_T = the thermopower voltage;

Equations 2 and 3 show that the signals reflected by different reflector networks have different phase characteristics. Short-circuit (SC) transmission-line voltage is a sinusoidal function, but open-circuit (OC) transmission-line voltage is a cosine function. Changing the type of transmission line can optimize the performance of the multiplier. The voltage of an SC transmission line can be found by studying Eq. 2, while the voltage of an OC transmission line can be calculated by Eq. 3:

$$V(d) = 2jV^{+}\sin(\beta d) \quad (2)$$
$$V(d) = 2V^{+}\cos(\beta d) \quad (3)$$

where:

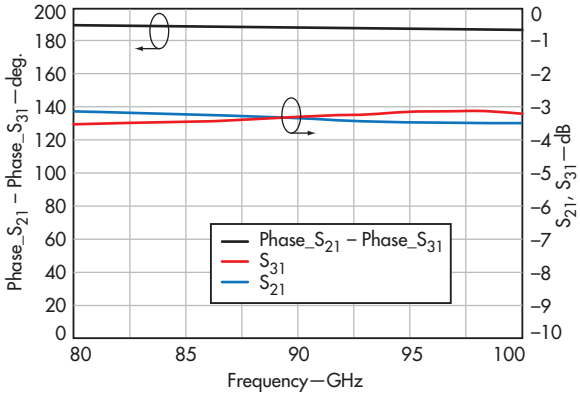
V^{+} = the voltage amplitude of the electromagnetic (EM) wave propagating along the positive direction;
β = the phase constant of the transmission line; and
d = the length of the transmission line.

As a result, it is necessary to optimize the input-power network and the input/output reflection networks to minimize the CL of a high-frequency multiplier design.

A Marchand balun is often part of the design of balanced multipliers, mixers, and amplifiers. The balun can be designed in a number of different ways,

with multiple planar balun structures proposed in ref. 9. The balun shown in *Fig. 2* offers a similar design. From a study of *Fig. 3*, it is possible to learn that (a) the phase difference (P2 minus P3) is 185 to 190 deg. between 80 to 100 GHz and (b) the insertion loss (from P2 to P1 and from P3 to P1) is less than 3.6 dB from 80 to 100 GHz.

The input-power network and the input/output reflector networks can be optimized with the assistance of computer analysis using the Advanced Design System (ADS) software from Agilent Technologies (www.agilent.com) and load-pull technology for analysis. It is well known that the output port of a balanced frequency multiplier will only contain even-harmonic signals and, according to the nonlinear characteristics of the multiplier, the impact of CL is weak on the higher multiplied harmonic signals. So, analysis at the input port of the multiplier can focus on the input power, the fundamental-frequency signals, and the second- and fourth-harmonic signal impedance at the multiplier's input port. In addition, the second-, fourth-, and sixth-harmonic impedances at the output port of the multiplier should also be studied. The input and output reflector networks for the multiplier include SCs, OCs, and matching circuits (MCs).



3. The simulated phase and insertion loss for the balun are plotted versus frequency.

Table 1 provides data for analysis of CL performance for different networks, with a number of conclusions possible by examining the table. For one thing, a change of CL impacted by the second- or fourth-harmonic reflector networks at the input port is about 0.1 dB, and this can be ignored. The appropriate input fundamental-frequency power reduces the VCL

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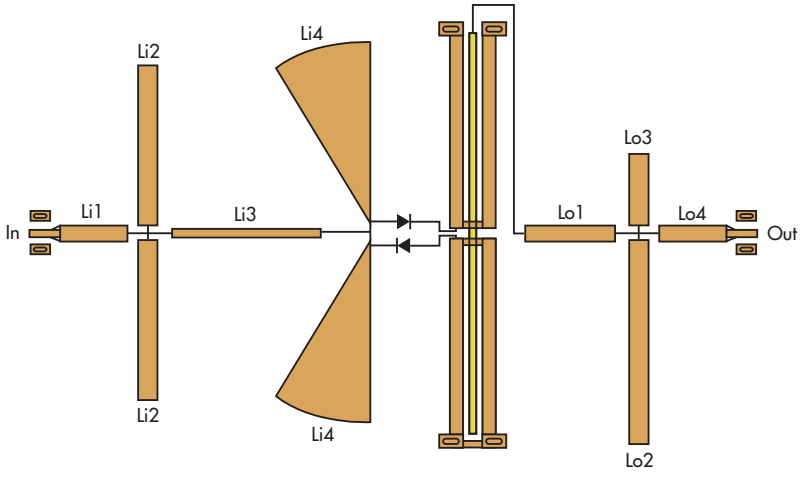
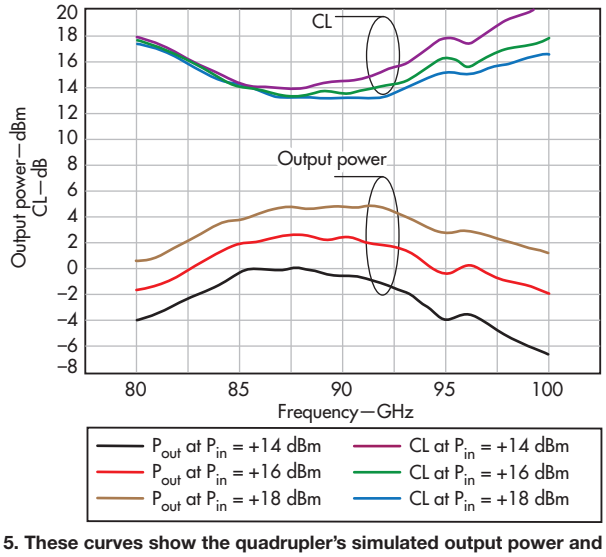


4. This diagram shows the optimized structure of the balanced quadrupler.

by about 1 dB, so the level of the fundamental input power should be a concern in the design of a frequency multiplier. When the second-harmonic reflector network is an open circuit at the output port, the CL is reduced by about 1 dB, which is an important consideration. Also, when the six-harmonic reflector network is an open circuit at the output port, the CL is reduced by about 0.2 to 0.4 dB, not a small amount of loss. According to these data, it is possible to optimize a Schottky diode multiplier for certain operating conditions. The specific structure is shown in *Fig. 4*.

As the studies show, a number of conclusions can be drawn. For one, the input reflector networks have been used to both impedance-match the fundamental-frequency signals and short-circuit the second- and fourth-harmonic signals. The output reflector networks are used to both impedance-match the fourth-harmonic signals and open-circuit the second- and sixth-harmonic signals. As shown in *Fig. 5* and *Table 2* (online only), the quadrupler's specific layout can be obtained by analysis of these matching requirements. By using commercial analysis software such as ADS, it is also possible to determine the output power (based on an input-power level) and the CL curves for a frequency-multiplier design. From such computer simulation curves, the maximum output power point and minimum CL point for the quadrupler is found to be near

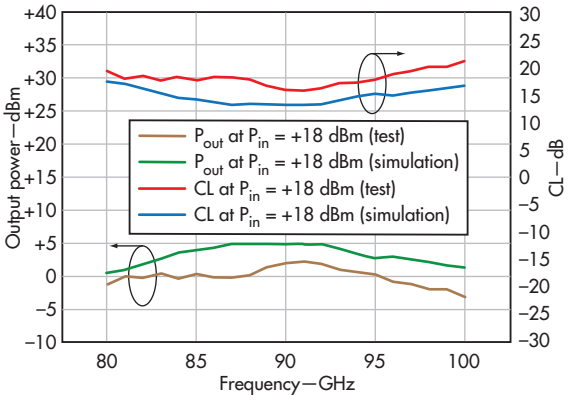


5. These curves show the quadrupler's simulated output power and conversion loss (CL).

87 GHz when the input power is around +20 dBm. The minimum CL is around 13 dB and the output power is around +7 dBm. This quadrupler design was realized with a 0.1-µm-gate-length GaAs pHEMT process *(Fig. 6)*.

The device was testing in a Class 10,000 cleanroom, measured on wafer using a model M150 probe station from Cascade Microtech (www.cmicro.com), a model ACP110-S ground-signal-ground (GSG) W-band probe from Cascade Microtech, and a model W8486A W-band power probe from Agilent Technologies. Simulated and measured results are compared in *Fig. 7*, showing that the output frequency characteristics between modeled and measured results are somewhat offset. This is most likely because since the quadrupler works at W-band frequencies, the Schottky diode model may not be totally accurate.

Still, it was possible to simulate the performance of a Schottky diode multiplier from 80 to 100 GHz with results that were fairly close to the measurements of an actual fabricated quadrupler for that same range. The analysis showed that it is possible to reduce the multiplier's CL, provided that the input-power network and the input/output reflector networks are fully optimized. The monolithic quadrupler that was finally fabricated can produce output levels of about −3 to +2 dBm across the target frequency range of 80 to 100 GHz. mw



7. These curves compare the measured and simulated performance with frequency for the quadrupler.

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6. This microphotograph shows the fabricated quadrupler.