RF POWER MOSFETS GET PUT TO THE VSWR TEST

TO ENSURE PROPER operation under real-world conditions, RF power MOSFETs undergo voltage-standing-wave-ratio (VSWR) testing to reveal considerable details about their failure modes. Such testing identifies device weakness while enabling a more rugged design. In "Application Note 1820: VSWR Testing of RF Power MOSFETs," Microsemi discusses these VSWR test failure modes as well as a new VSWR ruggedness test method.

Various load conditions produce three dominant failure modes under the VSWR testing of RF power MOSFETs. Over-voltage failure of either the periphery or die body can be avoided by using a nominal supply voltage fit for the amplifier circuit's class of operation. Thermal over-dissipation failure, which arises when the safe operating area (SOA) of the device is exceeded, is inevitable at some point of operation. This failure is a function of the inefficiencies of an amplifier under certain phases of the reflection coefficient of the load. Latch-up, which is sometimes difficult to distinguish from over-voltage failure, is a product of the bipolar elements within an RF power MOSFET and can cause device failure.

A typical VSWR test uses a gate and drain power supply to bias and power the device under test (DUT). A signal generator boosted by a power amplifier is often used to drive the DUT. To induce the various ranges of reflection, a load switch between a 50-Ω dummy load attenuator and RF power meter with a loss pad routed into a reactive load are used. To test latch-up, an unclamped-inductive-surge (UIS) test is performed using an inductor between the supply and drain voltage of the MOSFET. The inductor is charged while the gate is on. When the gate is switched off, the inductor surges power into the device.

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To de-embed the changes in efficiency and power dissipation in the test amplifier from the voltage breakdown failure, which results from VSWR testing, a 20% duty pulse of 200 μs can be used. For phase adjustment, a split variable capacitor in a tunable, dual-LC network could replace several lengths of coaxial line, which is the traditional approach. This method would enable the VSWR test to reach nearly 100% reflection efficiency with reasonable Q inductors at nearly any phase angle.

See "Microsemi VSWR - Load Mismatch Ruggedness" at www.youtube.com/watch?v=bMEsEATudgM.

DETAILED THERMAL MODELS BENEFIT IC PACKAGE DESIGNS

GENERATING HIGH-QUALITY PREDICTIONS of component temperatures can let circuit and package designers optimize their designs and avoid temperature-related failures. Various methods for thermally modeling components are available, and choosing the appropriate methods to balance simulation times and the fidelity of the prediction is a critical step. An application note by Mentor Graphics, "10 Tips For Predicting Component Temperatures… A High-Level 'How To' Guide," discusses the benefits of a detailed thermal model along with a step-by-step approach to predictive thermal modeling.

Choosing the appropriate method of modeling for each component in the design could optimize the prediction simulation timing, as well as allow for more detailed analysis of higher-profile components. To simplify the model, low-power density components may be described using background thermal profiles, where larger components that disrupt airflow may need to be modeled with 3D techniques. High-power and large components may need to be evaluated in a detailed discrete basis. Using good power estimates for these components in initial thermal planning could save significant time and effort costs later in the design cycle.

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A way to estimate the thermal effect of components early on when the final design is still nebulous is to use package thermal models, which can be increased in detail as the design progresses. Types of models include two-resistor, RC-ladder, DELPHI, and detailed. The thermal significance of the component often dictates the detail of the model. Sometimes, customized thermal models may be necessary. Using maps of the power distribution through the die could lead to more viable thermal predictions, along with calibrating model data using experimentally derived thermal profiles.

The final recommended steps consider heatsink solutions, thermal interface material (TIM) resistance, and thermal profiles of mechanical stress prediction. Design considerations like pressure drop, the wake region formed by the heatsink, and increased contact area could lead to a custom solution being more thermally viable for the design. The thermal resistance of the TIM could be a significant contributor of junction temperature, and a quality thermal prediction could lead to a suitable TIM choice. Finally, thermally induced stress on the packaging and substrate of the die based on the application environment may be critical in design decisions.