

LNA Integrates Fast Shutdown Function

This low-noise amplifier includes an on-board switching function with industry-leading switching speed, thus reducing dead time when a transceiver shifts between transmit and receive modes.

Time can be critical in modern communications systems, such as time-division-duplex (TDD) wireless systems. Although frequency-division-duplex (FDD) approaches have long dominated cellular communications, limited spectrum and high cost are making TDD approaches more attractive, as evidenced by growing use of standards such as time-division synchronous code-division-multiple-access (TD-CDMA) and TD Long Term Evolution (LTE).^{1,2} To prevent dead time in TDD switching, reception should ideally commence as soon as transmission has ended.

However, a cellular system’s low-noise amplifier (LNA), which is typically shut down during transmission to prevent damage of active devices and receiver overload, can suffer delays in returning to its active state. Because of these delays, a “guard time” of about 2% of the channel time must be allocated as settling time for the wireless system’s hardware.³ When transmission recommences, any delay in shutting down the LNA can result in temporary receiver overload.

In older wireless system implementations, the shutdown function was external to the LNA device. To reduce parts count and enable miniaturization of the LNA, the amplifier and its shutdown function are now typically integrated in a monolithic microwave integrated circuit (MMIC). Such MMICs are commercially available with switching speeds ranging from one-half microsecond to several microseconds (Table 1).

To enable further reduction in TDD dead time, a MMIC LNA was developed with an on-chip switching circuit optimized for speed. In addition to switching speed, this new LNA design must also meet the stringent noise and linearity requirements demanded by the cellular infrastructure.

In designing this MMIC LNA with faster shutdown speed, the location of the switch location within the circuit can influence the switching speed and affect the ease of integration for the device. A shutdown function can be added to virtually any MMIC by connecting a switching transistor in series with the voltage supply, V_{dd} (Fig. 1). The transistor’s current-carrying capability must match the MMIC’s current consumption, typically ranging from tens to hundreds of milliamperes. The single-supply MMIC design of Fig. 1 generates its gate bias (V_{GS}) using voltage reference V_D .

Diode resistance R_D limits the current through diode D. The forward-biased diode generates wideband noise and capacitance C is required to suppress that noise. Unfortunately, this capacitance requires a finite amount of time to charge and discharge.

TABLE 1: COMPARING ON/OFF TIMES FOR VARIOUS SWITCHED MMIC LNAs

Reference	Technology	On time, t_{on} (µs)	Off time, t_{off} (µs)
16	SiGe	8.5	5.0
17	0.5-µm eHEMT	0.5	0.5
18	GaAs HBT	0.4	0.3
19	0.25-µm ePHEMT	0.6	unknown
20	unknown	1.4	0.4
21	unknown	1.4	0.4
Current	0.25-µm ePHEMT	0.05	0.02

The time constant associated with $R_D C$ slows the rise time of the gate voltage V_{GSat} with power on, while $R_G C$ delays gate bias V_{GS} from decaying to zero at shutdown.

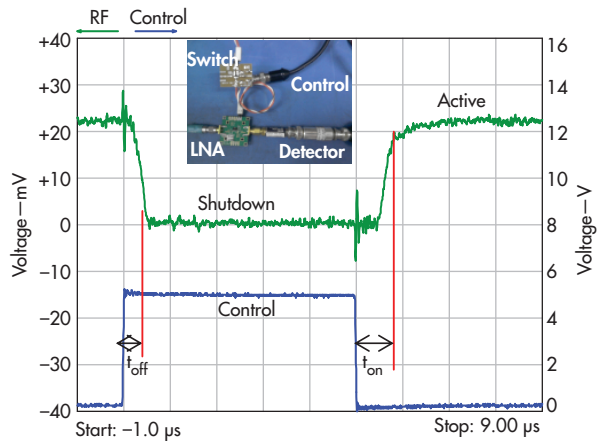
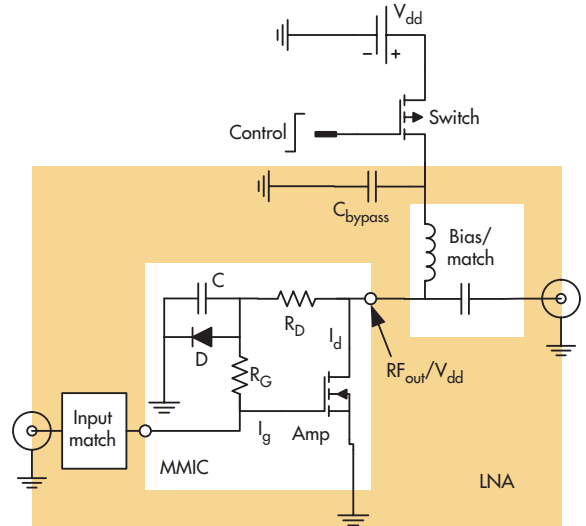
Additionally, the combination of the supply bypass capacitor C_{bypass} and the switching transistor's "on" resistance (typically 25 to 200 Ω^4) can also slow down the switching speed, particularly if a large value of C_{bypass} is chosen to effectively suppress supply transients. Because of these unavoidable time constants, an externally switched MMIC LNA will be limited in switching speed. Typical switching speeds range from 1 to 4 μs (Fig. 1).⁵

The MMIC is fabricated by means of a proprietary 0.25- μm enhancement-mode pseudomorphic high-electron-mobility-transistor (ePHEMT) process on 6-in. wafers.^{6,7} The MMIC integrates dual amplifiers, adjustable active biasing, and shutdown functions housed in a 16-pin 4 \times 4 \times 0.85 mm quad-flat-no-lead (QFN) package.^{8,9} A cascade configuration (Q4-5) was chosen for the amplifier because one common-source stage cannot meet the target gain at S-band (Fig. 1).

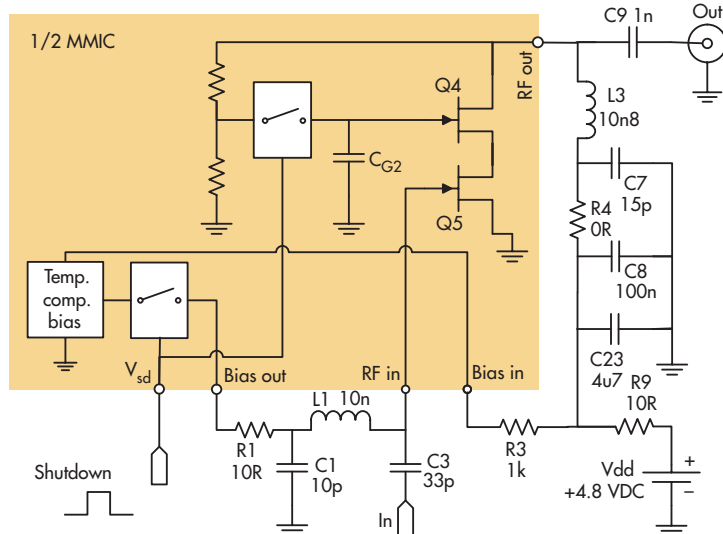
The cascade configuration's bottom gate is biased by a temperature-compensated voltage reference and the top gate is biased by a resistor divider. During shutdown, both gates are disconnected from their respective biasing sources by internal transistor switches. Because gate current is in the microampere range, small switching transistors can be used for this purpose. Although interrupting either one of the two gate supplies is sufficient to shut down the cascade amplifier configuration, switching both gates simultaneously improves the forward isolation and the switching speed of the LNA switch function.

Because the switches are fabricated on the same high-speed process as the RF amplifier, their propagation delays are small in comparison to the overall switching time. On the other hand,

2. This monolithic integration of the LNA shutdown function reduces the parts count and the switching time.

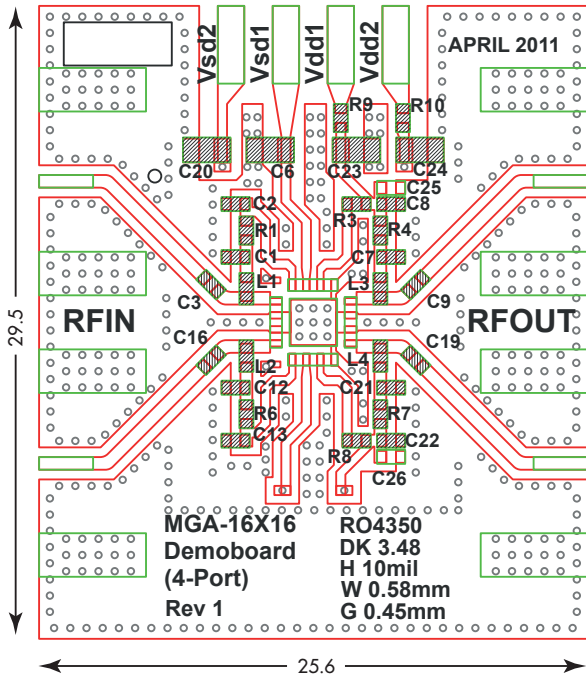


1. This shutdown function can be adapted to any LNA by inserting a switch into the supply line, but it will be limited to switching speed of no faster than 1 μs .



the RC components, required to bias and decouple the cascode gates, can slow down the switching speed through their time constants. Since the biasing components are necessary, the only way to mitigate their effect on the switching speed is to choose the smallest usable values for capacitances C_1 and C_{G2} and the connected resistances.

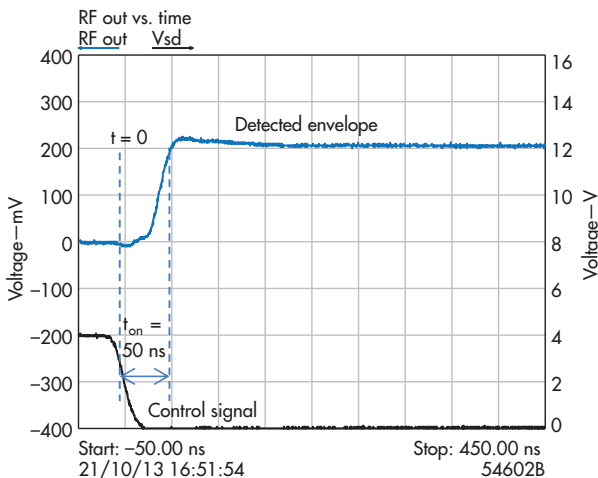
In contrast to the externally switched example (Fig. 1), the monolithic integrated shutdown function permits large-value capacitances to be used for bypassing the supply (e.g., C_8 and C_{23}) without sacrificing switching speed; larger value capacitances confer greater immunity to supply transients.¹⁰ The cascode's input and output impedances are matched by L_1 and C_3 and L_3 and C_9 , respectively. These components form highpass LC networks and are dimensioned for operation at 2.6 GHz, i.e., the UMTS VII



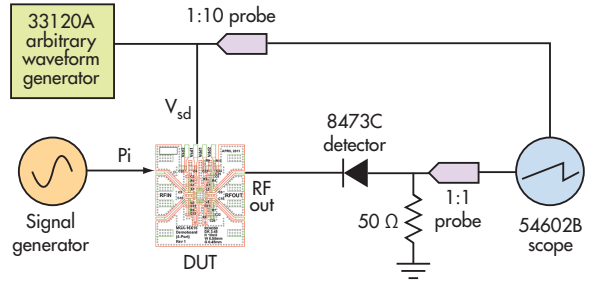
3. Two independent LNAs with shutdown functions fit on this compact PCB.

band.¹¹ The supply voltage V_{dd} is +4.8 VDC and the current is about 55 mA.

The prototype LNA was assembled on 10-mil-thick Rogers RO4350B printed-circuit-board (PCB) material from Rogers Corp. (www.rogerscorp.com), where 50-Ω microstrip traces are 0.58 mm wide (Fig. 3). The RO4350B material has a dielectric constant of typically 3.48 in the z-direction at 10 GHz. An FR-4 backing layer provides rigidity and increases the stack height to 1.6 mm to suit edge-launch SMA receptacles.



5. The prototype switched LNA exhibited turn-on time of only 0.05 μs.



4. This simple block diagram shows the test setup for measuring the LNA's switching speed.

MAKING MEASUREMENTS

The time taken to switch from one LNA state to another has been variously referred to as “switching time/speed/rate” and “power settling time” due to absence of a standardized terminology. The turn-on time, t_{ON} , is measured from 50% of the control signal to 90% of the final output amplitude.^{12,13} The turn-off time, t_{OFF} , is similarly defined. The setup (Fig. 4) for evaluating the LNA switching speed follows¹³ An RF signal generator feeds the LNA with a 2.6 GHz, 0-dBm carrier.

A pulse generator provides the logic-level control signal for the switches. The envelope of the amplified carrier is detected by a low-barrier Schottky diode detector. The output of the detector is loaded with a 50-Ω feedthrough resistor to quicken its response time to between 8 and 12 ns.¹⁴

As part of the switched-LNA test setup, an oscilloscope displays the detected envelope and the control signal; the rising/falling edge of the control signal triggers the oscilloscope. Although a spectrum analyzer can replace the combination of a diode detector and an oscilloscope, the latter was selected for its fast response time compared to a spectrum analyzer.¹⁵

Measurements of the prototype switched LNA show it to exhibit the fastest turn-on and turn-off times in the industry (Table 1).¹⁶⁻²¹ Since the LNA's switch control signal was used to trigger the oscilloscope, the $t = 0$ positions in both oscilloscope graphs (Figs. 5 and 6) represent the midway point (50%) of its falling/rising edge. To “wake up” the dormant LNA, the control signal, V_{sd} , transitions from high to low (Fig. 5). The detected envelope, RF_{out} , which rises from 0 V to about 210 mV, corresponds to the change in the LNA's output amplitude. The experimental on time, t_{ON} , is 0.05 μs.

To shut down the LNA, the control logic voltage, V_{sd} , changes

TABLE 2: SIZING UP OTHER KEY SWITCHED LNA PERFORMANCE PARAMETERS			
Gain (dB)	Noise figure (dB)	Power at 1-dB compression (dBm)	Third-order intercept point (dBm)
18.4	0.6	+18.0	+33.0

level from “LOW” to “HIGH” (Fig. 6). Correspondingly, the detected envelope, RF_{out} , decreases from about 200 mV to 0 V. Referenced to the control-signal midpoint, the detected envelope (RF_{out}) requires 0.02 μ s to drop to 10% of its maximum value.

The actual t_{OFF} time is most likely faster than the experimental value of 0.02 μ s because it is very close to the diode detector’s specified response time ($\leq 0.012 \mu$ s). In addition to speed, the prototype switched LNA exhibited excellent performance levels in various other parameters, as detailed in Table 2.

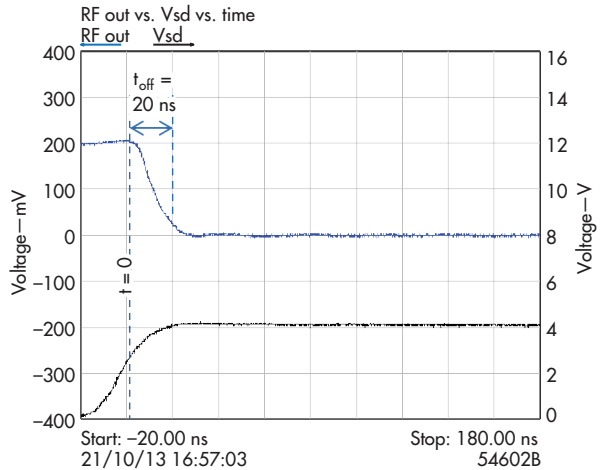
In conclusion, this integration of the shutdown function with the LNA circuitry avoids the high current levels and slower speeds associated with external switching solutions. A combination of fast pHEMT technology, dual switches, and optimum circuit connections enable this design to be more than one order magnitude faster than its closest competitor. **mmw**

ACKNOWLEDGMENTS

The author would like to thank H.A. Zulfa and Y.H. Chow for the IC design; S. Punithvati and M.D. Suhaiza for assembling the prototypes; and S.A. Asrul and the management of Avago Technologies for approving the publication of this work.

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