Product Feature

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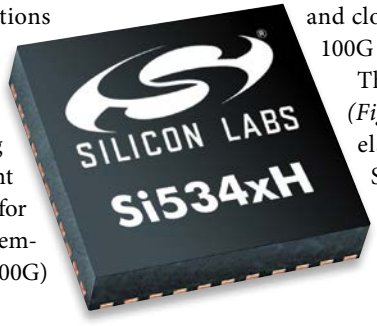
Clocks Attenuate Jitter in Coherent Optical Systems

Using a combination of frequency-generation technologies, this pair of low-jitter clocks provides the clean outputs needed to drive data converters in coherent optical transceivers.

BANDWIDTH IS ESSENTIAL to any communications network, with the need for bandwidth growing as more users communicate on worldwide networks. With voice, video, and data being moved from place to place, the need for speed is driving network operators to pursue faster, more efficient networks. In fact, once standards were established for 100-Gb/s (100G) Ethernet networks, the debate seemingly began about requirements for a 400-Gb/s (400G) Ethernet standard.



1. The Si534xH series of coherent optical clocks accept inputs from 8 kHz to 750 MHz and provide outputs to 2.75 GHz in high-frequency mode.

Such high data rates typically call for optical communications systems, and those systems require precise clocks for timing and synchronization. To meet the needs of present 100G and future 400G Ethernet in wireless infrastructure, data-center-interconnect (DCI), metro, and long-haul networking equipment, Silicon Labs developed its Si534xH coherent optical clock family.

Boasting output frequencies as high as 2.75 GHz, these devices provide near jitter-free operation in support of coherent optical-fiber communications networks. With unparalleled frequency flexibility and multiple outputs, these clocks are candidates to replace much larger clock trees based on high-frequency voltage-controlled surface-acoustic-wave (SAW) oscillators (VCSOs) for such applications as data-converter clocking in coherent optical transceivers.

Coherent optical communications has made a comeback, in large part, due to advances in digital signal processing (DSP) and field-programmable gate arrays (FPGAs), which provide the digital processing capabilities for implementing advanced modulation schemes such as quadrature phase shift keying (QPSK) in broadband optical cables. Digital techniques can also overcome the limitations of fiber chromatic dispersion and polarization-mode dispersion that haunted earlier versions of chromatical optical communications systems.

For any broadband optical communications network, timing and synchronization are important functions, and the Si534xH series of high-speed clocks minimizes phase noise and clock jitter to levels that permit reliable 100G network performance.

The Si534xH series of high-speed clocks (*Fig. 1*) currently consists of two models: the two-input, two-output model Si5342H and the two-input, four-output model Si5344H. Both accept inputs from 8 kHz to 750 MHz and provide outputs to 2.75 GHz. Suitable for transmit- or receive-side timing, they achieve impressively low root-mean-square (RMS) phase jitter of 50 fs for offsets from 1 to 40 MHz when operated in high-frequency mode.

Both models are based on the firm's fourth-generation DSPLL technology, which replaces discrete fixed-frequency PLLs with an innovative, frequency-flexible mixed-signal approach that combines a low-phase-noise analog VCO with a digital phase detector and DSP-intensive, all-digital loop filter. This architecture also leverages SiLabs' proven MultiSynth fractional-N frequency-synthesis technology to generate a wide combination of output frequencies with 0 ppm errors.

In addition to the high-frequency signals provided by the DSPLL architecture (*Fig. 2*), both devices support lower-frequency clock synthesis based on the firm's MultiSynth technology, capable of generating any frequency to 712.5 MHz. The typical phase jitter for these outputs is less than 150 fs for offsets from 12 kHz to 20 MHz. Output ports for the two devices can be configured for either of the operating modes.

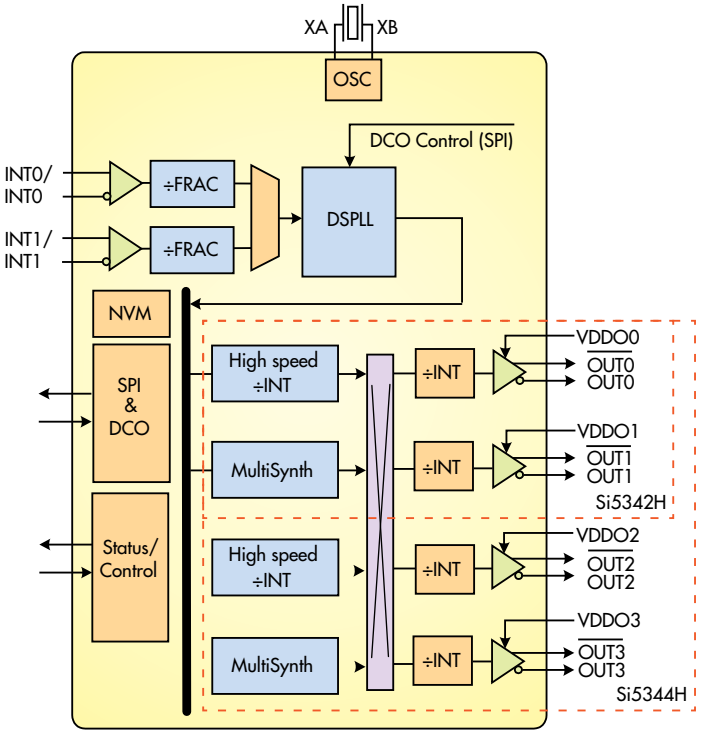
These coherent optical clocks employ frequency multiplication, fractional input dividers, and the internal DSPLL circuitry to produce low-phase-noise outputs from the provided input signals. They can even switch between input clocks without suffering hits, with input switching performed manually or automatically with an internal state machine. The DSPLL

circuitry can execute hitless switching between input clocks, even for two input clocks that are as much as ±500 ppm apart in frequency.

The amount of input clock jitter attenuation is controlled by the DSPLL loop bandwidth, with programmable loop bandwidths ranging from 0.1 Hz to 4 kHz. Since narrowband PLLs typically trade off longer lock acquisition times for greater jitter filtering at lower loop bandwidths, the Si534xH clocks offer a fast-lock mode that enables the devices to quickly acquire lock at a higher loop bandwidth and dynamically switch to a lower loop bandwidth once PLL lock is achieved.

In addition to the DSPLL circuit, both coherent optical clocks include MultiSynth dividers, capable of generating output signals that are integers or fractionally related multiples of the input signals for further signal-generation flexibility.

The Si5344H and Si5342H clocks include a digitally controlled oscillator (DCO) mode in which fast update rates can be achieved, and where all outputs are controlled simultaneously. This mode disables the outer loop of the dual-loop DSPLL circuitry to achieve updates that are essentially limited by the speed of the serial bus interface.



2. This block diagram shows the basic components within each of the two coherent optical clocks, and how different operating modes are achieved.

Both devices offer clock outputs that are highly configurable and can be programmed with specific voltage swings and for compatibility with a wide range of digital waveform standards. These include low-voltage positive emitter coupled logic (LVPECL), low-voltage complementary metal oxide semiconductor (LVCMOS), low-voltage differential signaling (LVDS), current mode logic (CML), and high-speed current-steering logic, although only LVPECL is available in the high-frequency mode.

The two clocks feature fast warmup time, with typical startup of 30 ms from power on to providing free-running output signals with stability based on an external reference oscillator. Both the Si5342H and the Si5344H devices are designed to provide precise frequency multiplication of supplied input signals and work with a simple, low-cost fundamental mode crystal. Due to the PLL design of these clocks, the best jitter performance is obtained with a crystal reference source from 48 to 52 MHz. A frequency-adjustment feature provides an adjustment range of ±200 ppm to correct for frequency offsets.

The devices offer multiple operating modes, including free-run, lock-acquisition, locked, and holdover modes. In free-run mode, the frequency accuracy of the output clock signals depends on the frequency accuracy of the external crystal or reference clock. The frequency accuracy of the output signals will match the accuracy of the reference. When high accuracy is needed in this operating mode, a high-stability oscillator, such as a temperature-controlled crystal oscillator (TCXO), may be used.

In lock-acquisition mode, input signals are monitored for a valid clock signal. After a selected input clock is validated, the DSPLL will automatically start the lock-acquisition process. In locked mode, the DSPLL generates output signals that are frequency- and phase-locked to the selected input clock. Once this is achieved, any input crystal-oscillator frequency drift will not affect the accuracy of the output frequency.

These devices will enter holdover mode when the selected input clock becomes invalid and a valid clock is not available on the other input. At that point, the DSPLL uses an averaged input-clock frequency as its holdover frequency to minimize degradation of the output-clock phase and frequency. The holdover circuitry stores as much as 120 s of historical frequency data while locked to a valid clock input, for use in holdover mode.

Both devices are programmed by means of a serial interface—either a serial peripheral interface (SPI) or I^2C interface. The ICs contain on-board nonvolatile memory that is read upon power-up, allowing the clocks to power up with a preprogrammed frequency configuration, simplifying device startup. They operate on core voltages of +1.8 and +3.3 V dc and include independent output supply pins for voltages of +3.3 V dc, +2.5 V dc, and +1.8 V dc.

Users can work with the firm's ClockBuilderPro software to program either device or choose factory-preprogrammed devices for known applications. Both clocks are built with lead-free and RoHS-compliant manufacturing processes and are designed for operating temperatures from −40 to +85°C. They are both supplied in 7- × 7-mm, 44-lead QFN packages. mw