# Board Packs Pair of Superhet Channels

## This low-power, wideband receiver module provides as much as 80 MHz for each of two superheterodyne channels with wide dynamic range from 10 MHz to 6 GHz.

Modularity often is synonymous with flexibility—a trait exemplified in the TwinRX daughterboard for the USRP X Series of software-defined radios (SDRs) from Ettus Research, a National Instruments company (www.ettus.com). Two of the TwinRX daughterboards fit within a model USR-PX300 or USRPX310 SDR, each of which measures just 27.7 × 21.8 × 3.9 cm and weighs a mere 1.7 kg.

The TwinRX daughterboards deliver 80-MHz bandwidth per receiver channel across a total frequency range of 10 MHz to 6 GHz. Thanks to their low noise figure and wide dynamic range, they support applications in commercial, industrial, and military areas, including signal intelligence (SIGINT) and passive radar systems to 6 GHz.

The compact TwinRX daughterboard *(Fig. 1)* is actually a full-fledged dual-channel receiver. The daughterboard is capable of local-oscillator (LO) sharing with other receiver daugterboards in a system for creation of multichannel receiver systems or even massive multiple-input, multiple-output (MIMO) system solutions. Each TwinRX dual-channel receiver is a low-power subsystem, with stable preselection filters *(Fig. 2)*, attenuators, and two frequency mixer stages with tightly controlled phase synchronization for effective use in spectrum monitoring and direction-finding (DF) applications.

### BROAD FUNCTIONALITY

The TwinRX achieves a 110-dB dynamic range at 2.4 GHz, 5.5-dB minimum noise figure at the same frequency, and only 10-W power dissipation. Each of the daughterboard's receiver channels has instantaneous bandwidth of 80 MHz that can be tuned independently across the full frequency range from 10 MHz to 6 GHz to capture and analyze a variety of signals in multiple-frequency bands of interest.

As an example, a single TwinRX daughterboard can simultaneously monitor uplink and downlink communications signals across a combined bandwidth of 80 + 80 = 160 MHz. By sharing LO signals across multiple TwinRX daughterboards, it is possible to achieve the phase-aligned operation needed for multichannel phased-array systems. In addition to the tight phase control, the dual-channel receiver is also capable of high-speed frequency-hopped tuning to detect frequency-agile emitters.

In terms of electrical performance, the dual-channel TwinRX exhibits noise figure of better than 5 dB from 10 MHz to 3 GHz, better than 4 dB from 3 to 5 GHz, and better than 8 dB from 5 to 6 GHz. Image rejection is –70 dBc from 0.5 to 6.0 GHz. The phase noise is –88 dBc/Hz offset 10 kHz from a 900-MHz carrier, –86 dBc/Hz offset 10 kHz from a 2.4-GHz carrier, and –82 dBc/Hz offset 10 kHz from a 5.8-GHz carrier. And phase noise is –105 dBc/Hz offset 100 kHz



**1. Each TwinRX daughterboard contains two independently tunable superheterodyne receiver channels for use from 10 MHz to 6 GHz.**

NORMALIZED PRESELECTOR FILTER RESPONSE
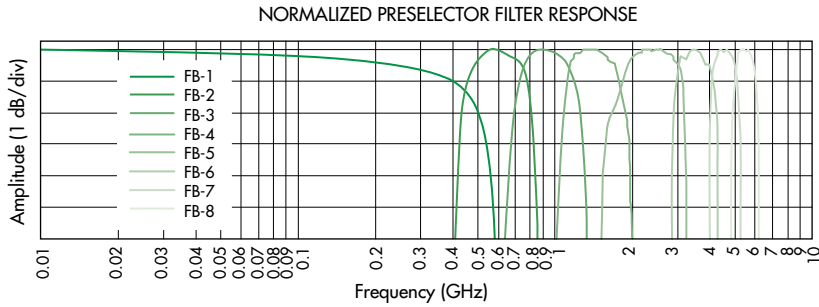


**2. Powerful preselector filter capability within each TwinRX dual-channel receiver allows for detection and isolation of signals from interference from 10 MHz to 6 GHz.**

from a 900-MHz carrier, –107 dBc/Hz offset 100 kHz from a 2.4-GHz carrier, and –103 dBc/Hz offset 100 kHz from a 5.8-GHz carrier.

In addition, non-input-related spurious levels are –95 dBc from 10 MHz to 3 GHz, –92 dBc at 3.2 GHz, –98 dBc at 4.8 GHz, and –98 dBc at 5.4 GHz. The third-order intercept point is –8 dBm for a full scale of –45 dBm from 10 MHz to 1.8 GHz, –2 dBm for a full scale of –30 dBm from 10 MHz to 1.8 GHz,

and +16 dBm for a full scale of –20 dBm from 10 MHz to 1.8 GHz, with similar readings at higher frequencies.

The TwinRX daughterboard and its host USRPX300 or USRPX310 SDR work with the USRP Hardware Driver (UHD) software to automatically configure radio settings to handle weak as well as strong signals. The USRP X300 and X310 SDRs offer multiple interface options, including PCIe and Dual 1/10 Gigabit Ethernet (GigE) interfaces. They are also designed around a Kintex-7 field-programmable gate array (FPGA) from Xilinx (www.xilinx.com) for programming flexibility.