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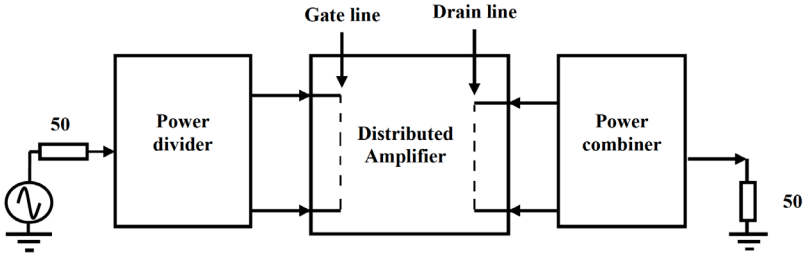
Apply a New Approach to Dual-Fed Distributed Amplifier Design

This novel design method helps improve gain for the dual-fed DA by approximating gain using the Chebyshev polynomial.

The topology of the balanced amplifier[1] allows for power to be added at the output. It's composed of two amplifiers, which may be multistage implementations, placed between the input power divider and the output power combiner *(Fig. 1)*. To enhance the design, a device known as the "Dual-Fed Distributed Amplifier" (DFDA), has been introduced.[2]



1. The DFDA amplifier configuration includes an input power divider and an output power combiner.

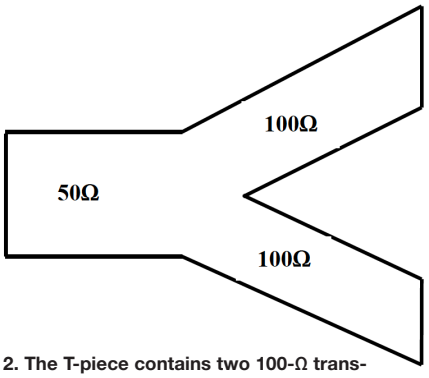
The operating principle of the DFDA involves injecting the signal to be amplified into both ends of the gate line. The output signal is recovered at the two ports of the drain line.

The DFDA is characterized by:[2]

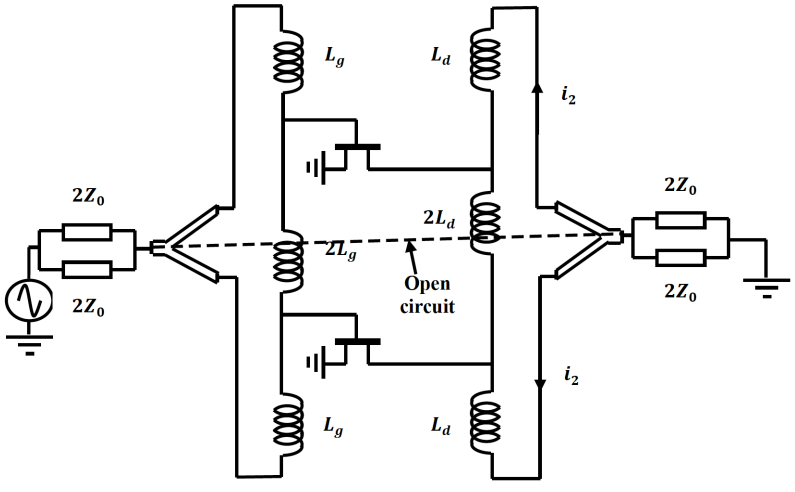
- A 6-dB increase in gain compared to the conventional distributed amplifier (CDA)[3] due to the direct and indirect gains being added. This is not the case with a CDA, in which only the direct gain is taken into account.
- A lower noise factor than that of the CDA due to the absence of the 50-Ω impedance at the ends of the gate and drain lines.

Using two transistors, it's possible to obtain an open-circuit line at the ends of the gate and drain lines.[4] While the gain improves, the bandwidth remains less than that of the CDA.

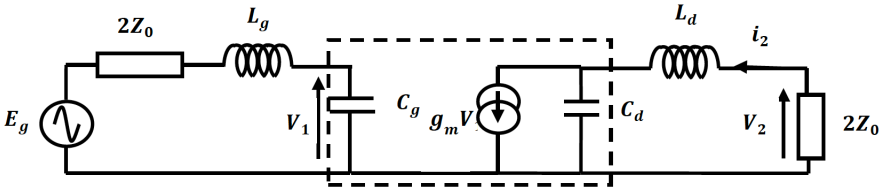
This article presents a new DFDA design technique that



2. The T-piece contains two 100-Ω transmission lines.



3. The MDFDA amplifier is symmetric in nature.



4. Shown is the equivalent MDFDA half-circuit.

allows for a stable gain over the entire bandwidth. The new amplifier is called a mismatched DFDA (MDFDA). The technique is based on the approximation of the amplifier transducer gain by the Chebyshev polynomial.

Amplifier Design

For this amplifier, the input and output power dividers are replaced by a simple T-piece composed of two 100-Ω transmission lines of unspecified length *(Fig. 2)*. The value of 100 Ω was chosen to match the input with the amplifier's gate line, as well as the output with the amplifier's drain line. The values of the components of the gate and the drain line are obtained by approximating the amplifier gain with the Chebyshev polynomial.

The amplifier diagram of *Figure 3* reveals a symmetric plane, meaning that such amplifiers are a product of the association of two identical half-circuits. Thus, the analysis of this type of amplifier will be based on that of a half-circuit.

The symmetric plane corresponds to an open circuit. Inductances are elements with constants localized; the equivalent diagram of the half-circuit is shown in *Figure 4*. This diagram is equivalent to that of the single-stage distributed amplifier (SSDA)[5] except that the source and load impedance values are doubled ($2Z_O = 100\ \Omega$).

To express the amplifier's transducer gain, we use the simple unilateral model of the MESFET transistor, shown inside the dashed line in *Figure 4*. Here, C_g and C_d are the gate and drain capacitances, respectively, of the field-effect transistor (FET) in common-source mode, while g_m is the transconductance. For this structure, the transducer gain, G_T, is:

$$G_T = \left. -\frac{1}{2} R_e(V_2 i_2^*) \right/ |E_g|^2 / 16Z_0 \qquad (1)$$

where V_2 and i_2 are the output voltage and current, respectively.

The transducer gain then becomes:

$$G_T = \frac{16Z_0^2 g_m^2}{[(1-4x^2)^2 + \alpha_1^2 x^2][(1-4a^2x^2)^2 + \alpha_2^2 a^2 x^2]} \qquad (2)$$

where $x = \omega/\omega_{c1}$ is the normalized frequency with respect to the cutoff frequency of the gate line. The other variables are defined as:

$$\omega_{c1} = 2/\sqrt{L_g C_g},\ \alpha_1 = 4Z_0/Z_{c1},\ \alpha_2 = 4Z_0/Z_{c2}$$

$$\alpha_2 = 4Z_0/Z_{c2},$$

and

$$a = \omega_{c1}/\omega_{c2}$$

Z_{c1} and Z_{c2} are the characteristic impedances at relatively low frequencies of the K-constant circuits constituting the gate and drain lines, respectively. They are defined as:

$$Z_{c1} = \sqrt{L_g/C_g}$$

$$Z_{c2} = \sqrt{L_d/C_d}$$

The cutoff pulsation of the drain line is:

$$\omega_{c2} = 2/\sqrt{L_d C_d}$$

We can then get the following results:

$$g_T = G_T/16Z_0^2 g_m^2 \qquad (3.1)$$

$$g_T = 1/(1 + A_2x^2 + A_4x^4 + A_6x^6 + A_8x^8) \qquad (3.2)$$

where:

$$\begin{cases} A_2 = a^2(\alpha_2^2 - 8) + (\alpha_1^2 - 8) \\ A_4 = 16a^4 + a^2(\alpha_1^2 - 8)(\alpha_2^2 - 8) + 16 \\ A_6 = 16a^4(\alpha_1^2 - 8) + 16a^2(\alpha_2^2 - 8) \\ A_8 = (16)^2 a^4 \end{cases} \qquad (3.3)$$

The approximation by the Chebyshev polynomial will be applied to the denominator of Equation 3.2. This approximation consists of writing the denominator of g_T in the $D = 1 + Q_n(x)$ form, or:

$$D = (1 - \varepsilon'^2)\left[1 + \varepsilon^2\left(1 + (Q_n(x)/\varepsilon'^2)\right)\right] \qquad (4)$$

Here, $\varepsilon^2 = \varepsilon'^2 / 1 - \varepsilon'^2$ represents the ripple ratio. We then carry out the approximation by using the Chebyshev polynomial of $T_n^2(x)$ of one part of the denominator as follows:

$$1 + \varepsilon^2\left(1 + (Q_n(x)/\varepsilon'^2)\right) = 1 + \varepsilon^2 T_n^2(x) \qquad (5)$$

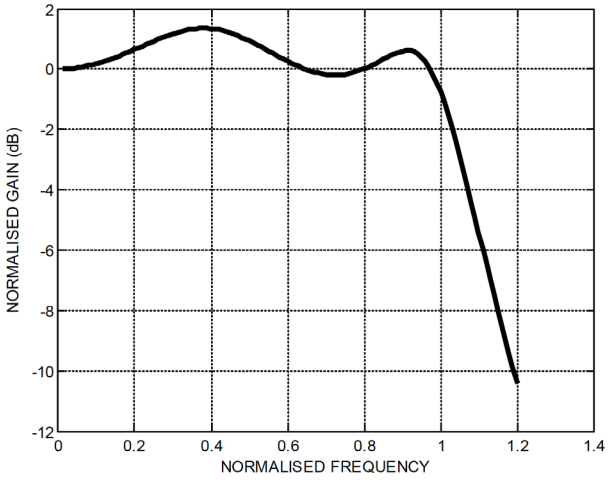
Therefore:

$$T_n^2(x) = 1 + (Q_n(x)/\varepsilon'^2) \qquad (6)$$

As $Q_n(x)$ is of the eighth degree, $T_n^2(x)$ must also be:[6]

$$T_n^2(x) = 64x^8 - 128x^6 + 80x^4 - 16x^2 + 1 \qquad (7)$$

After identification, Equations 3 and 7 imply the following set of equations:



5. Shown is the MDFDA's normalized power gain as a function of the normalized frequency.

$$A_8 = 64\varepsilon'^2$$
$$A_6 = -128\varepsilon'^2$$
$$A_4 = 80\varepsilon'^2 \qquad (8)$$
$$A_2 = -16\varepsilon'^2$$

where A_i *(i = 2, 4, 6, 8)* are the coefficients given by Equation 3.3.

Therefore, to design the MDFDA implementation, we must initially solve for the equations shown in the Equation 8 set, in which the roots are α_1, α_2, α, *and* ε'. The values taken by these roots are the same regardless of the characteristics of the FET used.

The resolution of equations in the Equation 8 set leads to the following result:

$$\alpha_1 = 2.38; \alpha_2 = 0.556; a = 0.511 \text{ and } \varepsilon^2 = 0.37 \qquad (9)$$

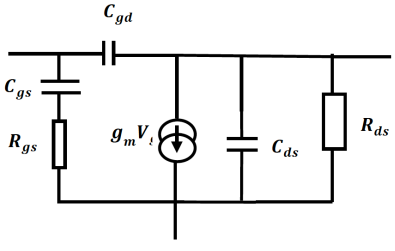
With the values of Equation 9 and by taking Z_O = 50 Ω, the design parameters as a function of the gate capacitance, C_g, can be derived as:

$$C_d = 0.13C_g;\ L_g = 7120C_g \text{ and } L_d = 15448C_g \qquad (10)$$

We then just need to know the value of C_g to proceed to the design of the amplifier.

The results given by Equations 9 and 10 are general and can thus be applied to any FET. Therefore, it's sufficient to only know the value of C_{gs} to proceed to the amplifier design.

Several points can be noted from the obtained results. The FETs with a value of C_d/C_g of less than 0.13 require a shunt capacitor to be added to the drain. The added capacitors combine with C_d to form a new capacitor, C_d', such that C_d'/C_g = 0.13. The shunt capacitor at the gate should be avoided, since it leads to a reduction of the bandwidth.



6. This is the equivalent circuit of a real transistor.

We can update the Equation 3.3 set and then Equation 3.2 with the values given in Equation 9 to calculate the normalized power gain as a function of the normalized frequency for the MDFDA amplifier. *Figure 5* reveals the calculated gain. The main characteristic is that this curve is universal. It should be noted that the MDFDA amplifier with a gain that's approximated by the Chebyshev polynomial achieves a stable gain over a large bandwidth. Here, the bandwidth is defined as a band of frequencies in which the gain is constant or has small variations.

Design and Simulation

We now will carry out the design and simulation of the amplifier studied previously. The internal parameters of the selected transistor are C_{gs} = 0.17 pF, C_{ds} = 0.006 pF, and g_m = 32 mS. The substrate chosen for the microstrip lines is characterized by its relative permittivity, ε_r, of 10.2. The height of the dielectric and the conductor thickness are 0.25 mm and 17 µm, respectively.

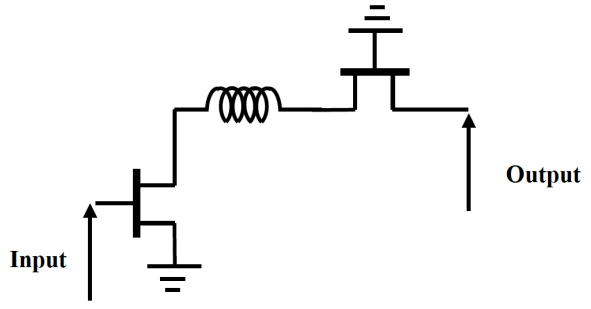
The TXLINE program within the Microwave Office design software was used to calculate the dimensions of the 100-Ω lines of the T-piece. Microwave Office software was used to perform all simulations.

The calculation of the widths (W) of the 100-Ω lines of the T-piece produced a value of 20.129 µm.

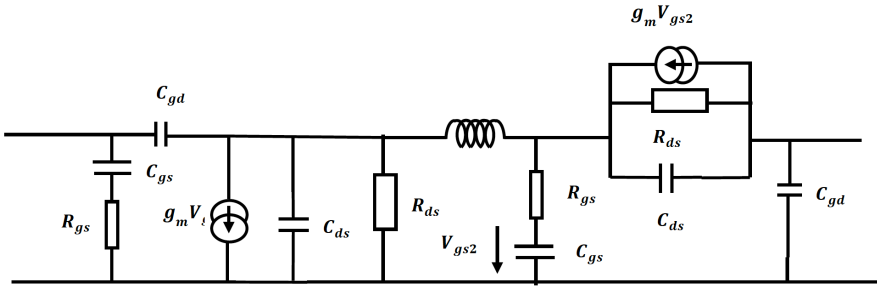
Using the equations shown in the Equation 10 set, we determine that L_g = 1210.4 pH, L_d = 2626.16 pH, and C_d = 0.0224 pF. The shunt capacitor with the addition of C_{ds} is:

$$C = C_d - C_{ds} = 0.022 - 0.006 = 0.016pF$$

The transducer gains of the MDFDA were simulated with Mi-



7. The cascode circuit contains an inductance between the transistors.



8. This circuit represents the equivalent of the cascode circuit.

crowave Office. The results are provided later in the article.

Using the Real Transistor Equivalent Circuit

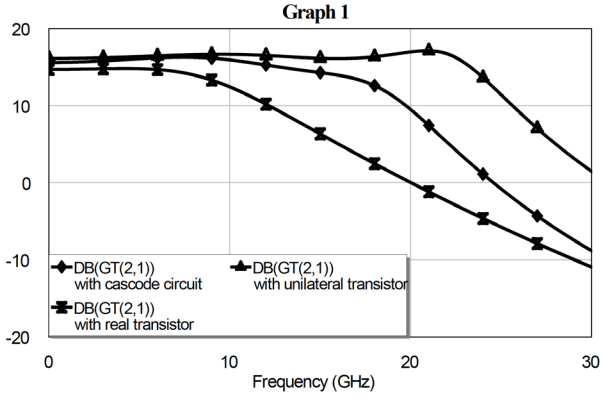
The study here assumed a unilateral transistor with an almost infinite capacitive output impedance value over the bandwidth considered. However, a real transistor does not achieve such characteristics. *Figure 6* shows an equivalent circuit of a real transistor. Here, C_{gd} = 0.016 pF, R_{ds} = 560 Ω, and R_{gs} = 0.53 Ω.

The circuit that's best suited for this study is the cascode circuit, in which an inductance is added between two transistors to reduce the effects of the input and output capacitances of the first and the second transistors, respectively, at high frequencies *(Fig. 7)*. *Figure 8* shows the equivalent circuit of the cascode circuit.

Ref. 5 reveals that, unlike a single-transistor circuit, the cascode implementation is a practically unilateral circuit that achieves an almost infinite output impedance. Thus, to design the MDFDA, we just need to replace the transistors in *Figure 3* with cascode circuits.

The shunt capacitor added at the output of the cascode circuit is equal to 0.006 pF. This is because we have the capacitor C_{gd} of the second transistor at the output of the cascode circuit. The value of the shunt capacitor is then calculated as:

$$C = C_d - C_{gd} = 0.022 - 0.016 = 0.006pF$$



9. Shown are the simulated gains of the MDFDA using a unilateral transistor, a real transistor, and the cascode circuit.

The value of the inductance (400 pH) between the two transistors of the cascode is obtained via optimization.

Figure 9 shows the simulated gains of the MDFDA using a unilateral transistor, a real transistor, and the cascode circuit. With a unilateral transistor, we can see that the gain is stable over the entire bandwidth. However, in reality, transistors are not unilateral, causing the gain and the bandwidth to decrease when using a real transistor versus a unilateral one. With the cascode circuit, we obtain good results—the gain of the amplifier is almost the same as the amplifier that employs a unilateral transistor.

Conclusion

This new design approach for the DFDA can apply to any MESFET transistor. The technique makes it possible to maintain a stable gain over a large frequency range due to the approximation of the amplifier gain by the Chebyshev polynomial. The design parameters can be determined in a very simple manner—one only needs to know the gate capacitance of the transistor. This approach allows for a distributed amplifier with substantial gain over a broad bandwidth.

References

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