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Feeds for Microstrip Array
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Deliver a Range of Semiconductor
Speeds and Frequencies **p51**

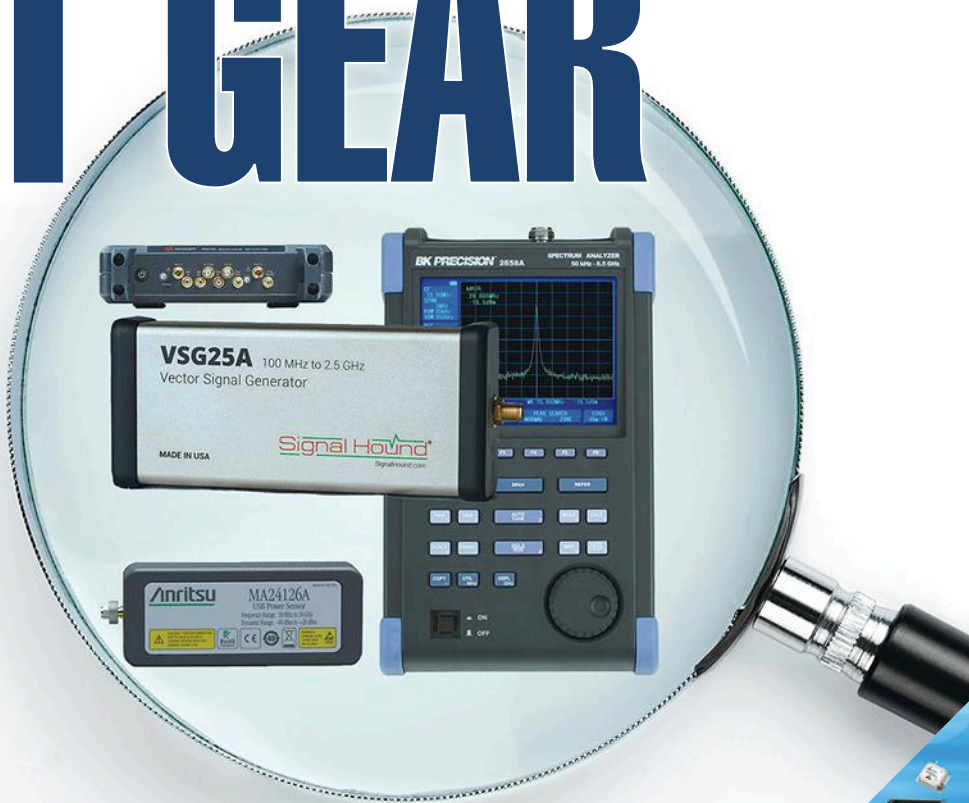
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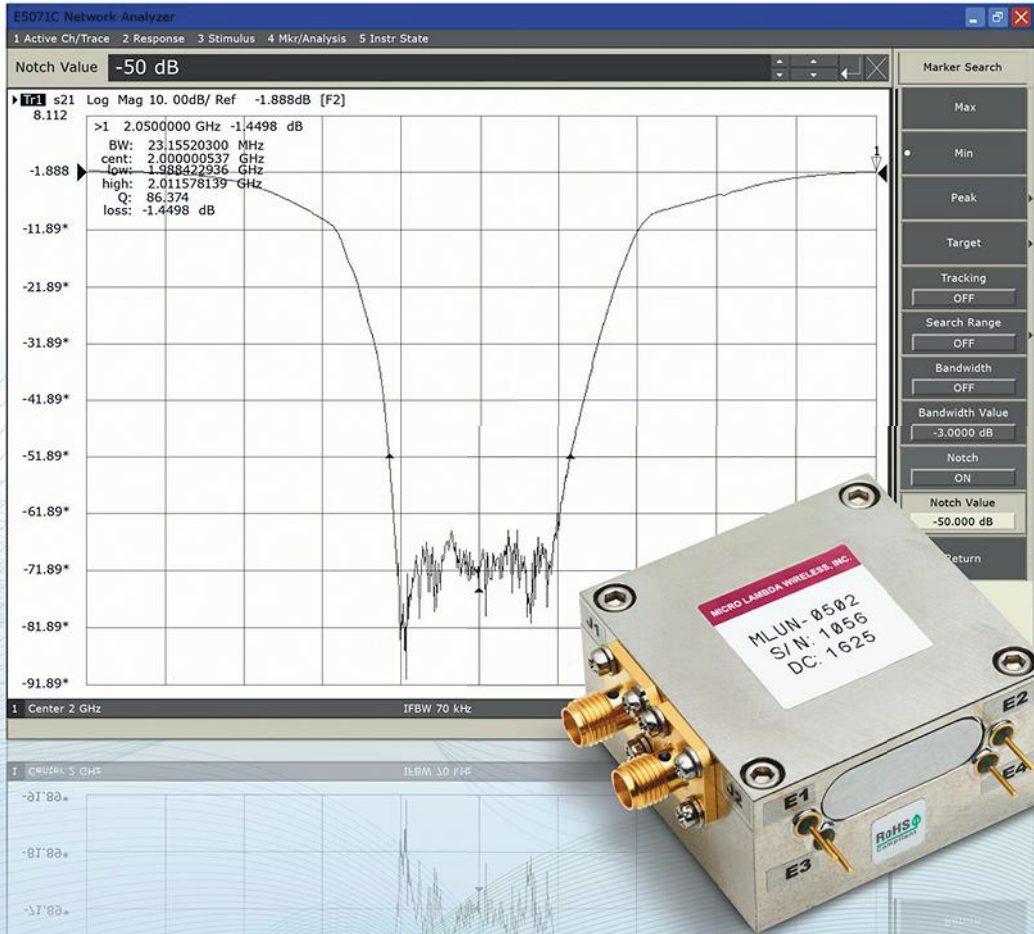


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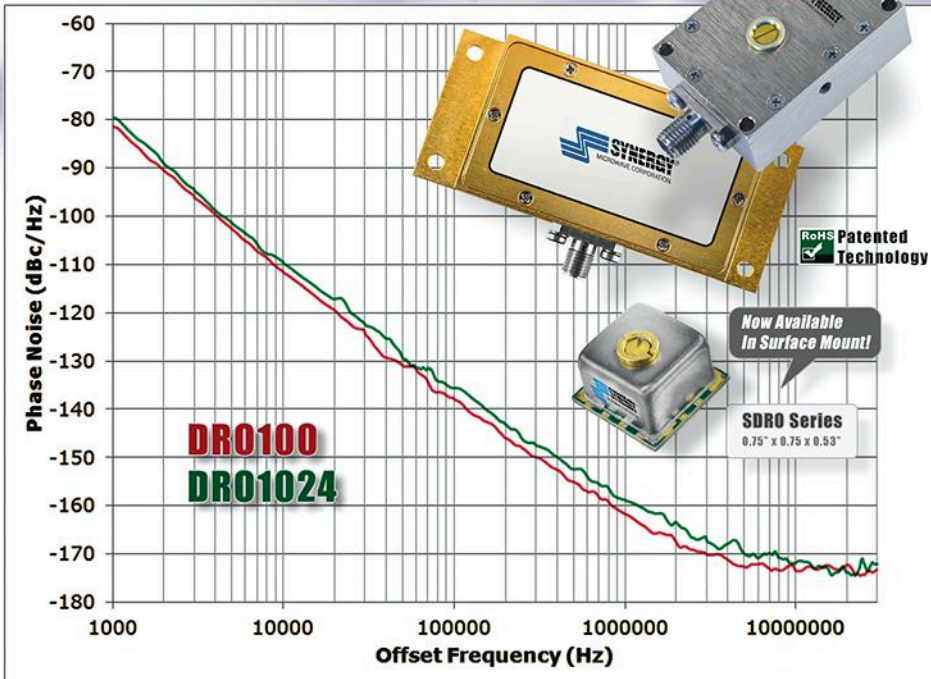
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SDRO1121-7	11.217	1 - 12	+5.5 - +7.5 @ 25 mA	-104
SDRO1130-7	11.303	1 - 12	+5.5 - +7.5 @ 25 mA	-104
SDRO1134-7	11.340	1 - 12	+5.5 - +7.5 @ 25 mA	-104
SDRO1250-8	12.500	1 - 15	+8.0 @ 25 mA	-105
Connectorized Models				
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DRO100	10.000	1 - 15	+7.0 - +10 @ 70 mA	-111
DRO1024	10.240	1 - 15	+7.0 - +10 @ 70 mA	-109
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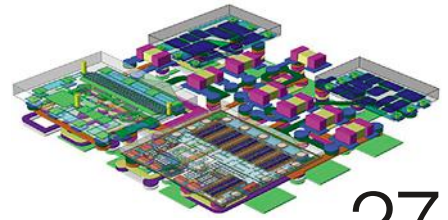


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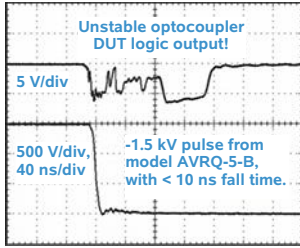
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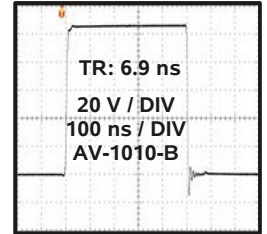
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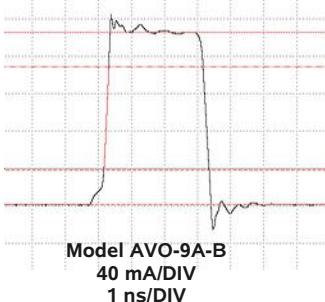
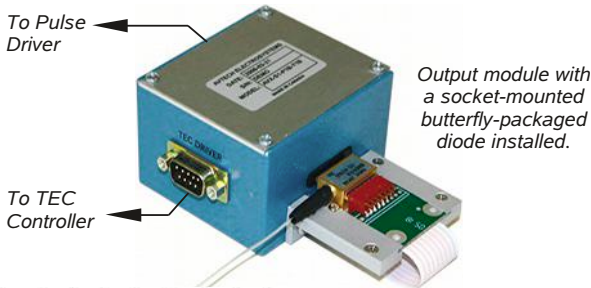
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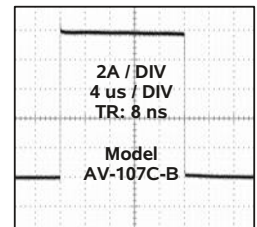
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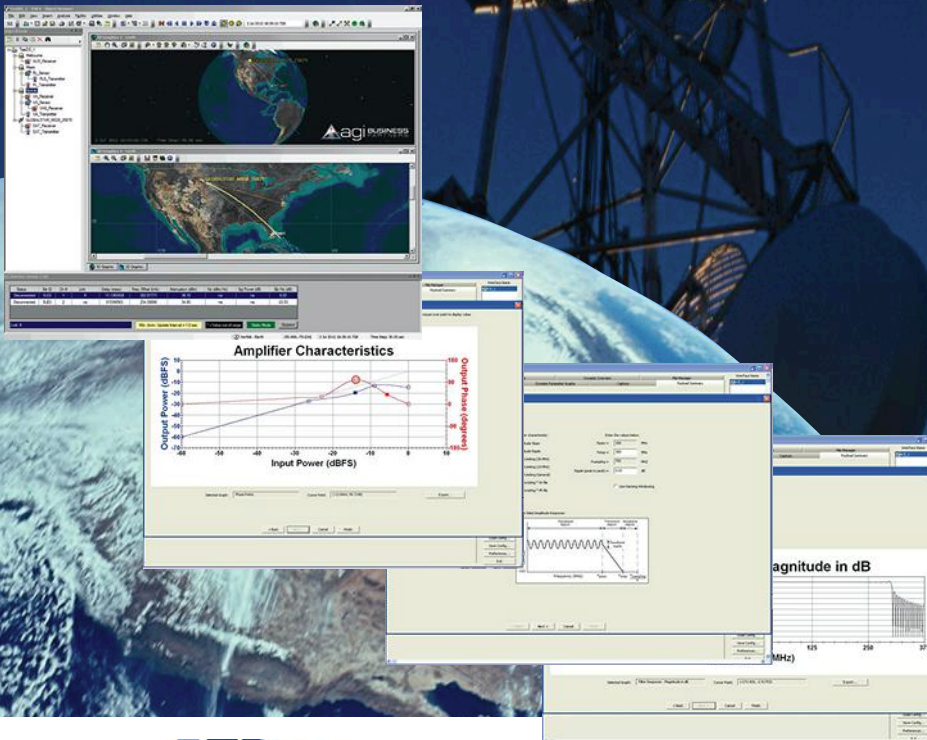
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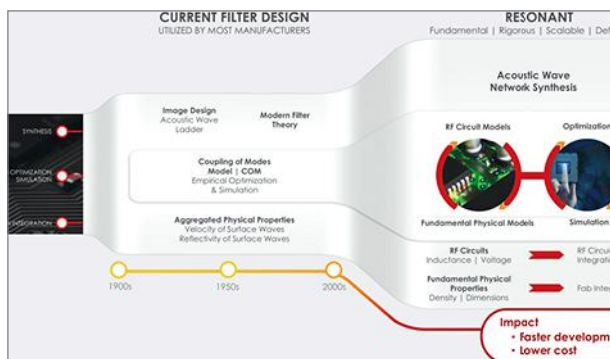
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How is this Company's Technology Enabling New Markets?

In this Q&A, Abhishek Kapoor talks about his new position with Anokiwave, the company's goal of commercializing active antennas for 5G and other applications, and more.

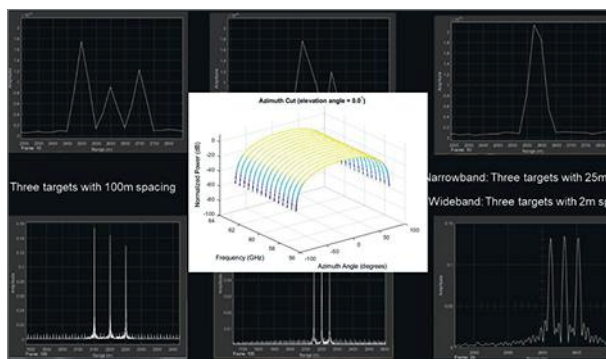
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Topics of interest include:

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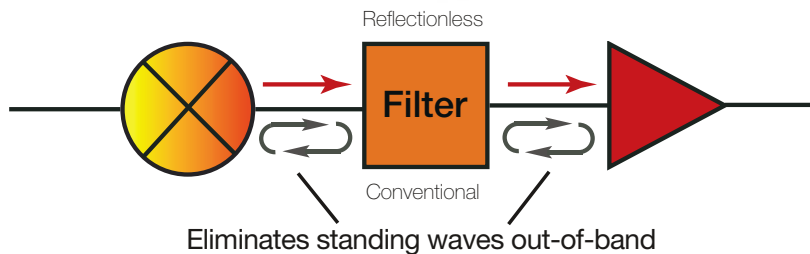
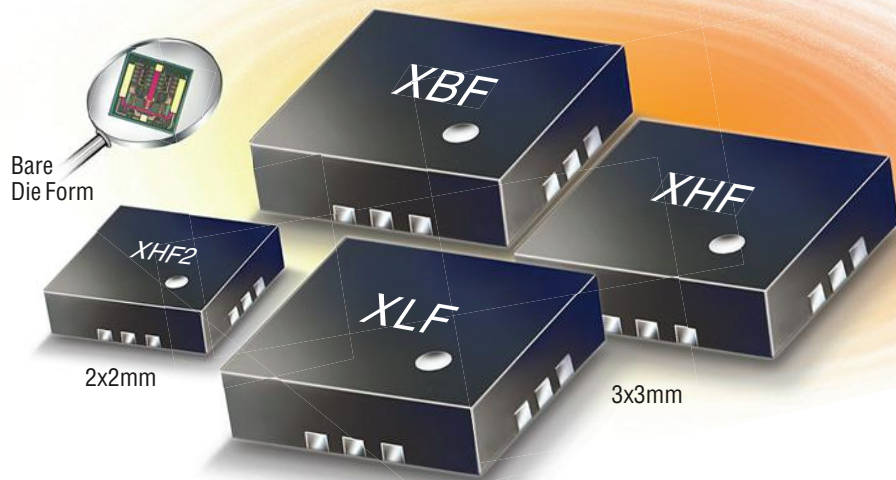


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Editorial

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Hits the 20-Year Mark

It's no secret that the IEEE International Microwave Symposium (IMS) is this industry's most significant event each year. But that doesn't mean you should overlook the other smaller conferences dotting the schedule throughout 2019. One industry event that may not pack the same punch as IMS, but is still noteworthy in its own right, is the annual IEEE Wireless and Microwave Technology Conference (WAMICON; www.wamicon.org). This year's installment, which marks WAMICON's 20th anniversary, is set to take place April 8-9 in Cocoa Beach, Fla.

WAMICON has come a long way—it started as a one-day forum, but is now a multi-day international IEEE conference. For WAMICON 2019, the theme is “Simulation Driven Design of Emerging Wireless, Microwave, and mm-Wave Circuits and Systems.”

As the theme indicates, simulation software will take the spotlight at this year's conference. Not only will tutorials be given by representatives from various simulation software companies, but a panel session will dive into emerging simulation technologies. Anyone interested in the latest developments creating a buzz within the simulation software arena may want to take note.

Of course, you can't talk about a conference without mentioning the keynote. WAMICON 2019's keynote speaker



will be Dr. Robert Weigel, professor at Friedrich-Alexander University Erlangen-Nürnberg. His presentation is titled, “Design and Simulation of Advanced Packaging Platforms for High Volume RF System Applications.”

In addition, Todd Cutler, vice president and general manager of design and test software organization at Keysight Technologies (www.keysight.com), will serve as the plenary speaker. The title of his presentation is “The Future of High-Frequency Test and Measurement.” I had previously written about Cutler's keynote at EDI CON 2016—“High-Frequency, High-Speed Design Revolution Ahead: Why Your Design and Test Flow Will Soon Be Obsolete.” It could be quite intriguing to hear his take on how the industry has evolved since then.

In addition to the various presentations and tutorials, several companies will be exhibiting at WAMICON 2019. They include Keysight, Wolfspeed (www.wolfspeed.com), Modelithics (www.modelithics.com), Copper Mountain Technologies (www.coppermountaintech.com), and several others.

Lastly, one of the nice things about WAMICON is simply the location. It takes place at the Hilton Cocoa Beach oceanfront hotel, which is certainly a nice place to have a conference! If you haven't already, you may want to pencil in WAMICON 2019 on your calendar. **mw**

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LS0560 P40B	0.5 - 6.0	1.3	1.5:1	+21
LS05012P40B	0.5 - 12.0	1.7	1.7:1	+21
LS1020 P40B	1.0 - 2.0	0.6	1.4:1	+21
LS1060 P40B	1.0 - 6.0	1.2	1.5:1	+21
LS1012P40B	1.0 - 12.0	1.7	1.7:1	+21
LS2040P40B	2.0 - 4.0	0.7	1.4:1	+20
LS2060P40B	2.0 - 6.0	1.3	1.5:1	+20
LS2080P40B	2.0 - 8.0	1.5	1.6:1	+20
LS4080P40B	4.0 - 8.0	1.5	1.6:1	+20
LS7012P40B	7.0 - 12.0	1.7	1.7:1	+18

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Note: 2. Typical limiting threshold: +6 dBm.

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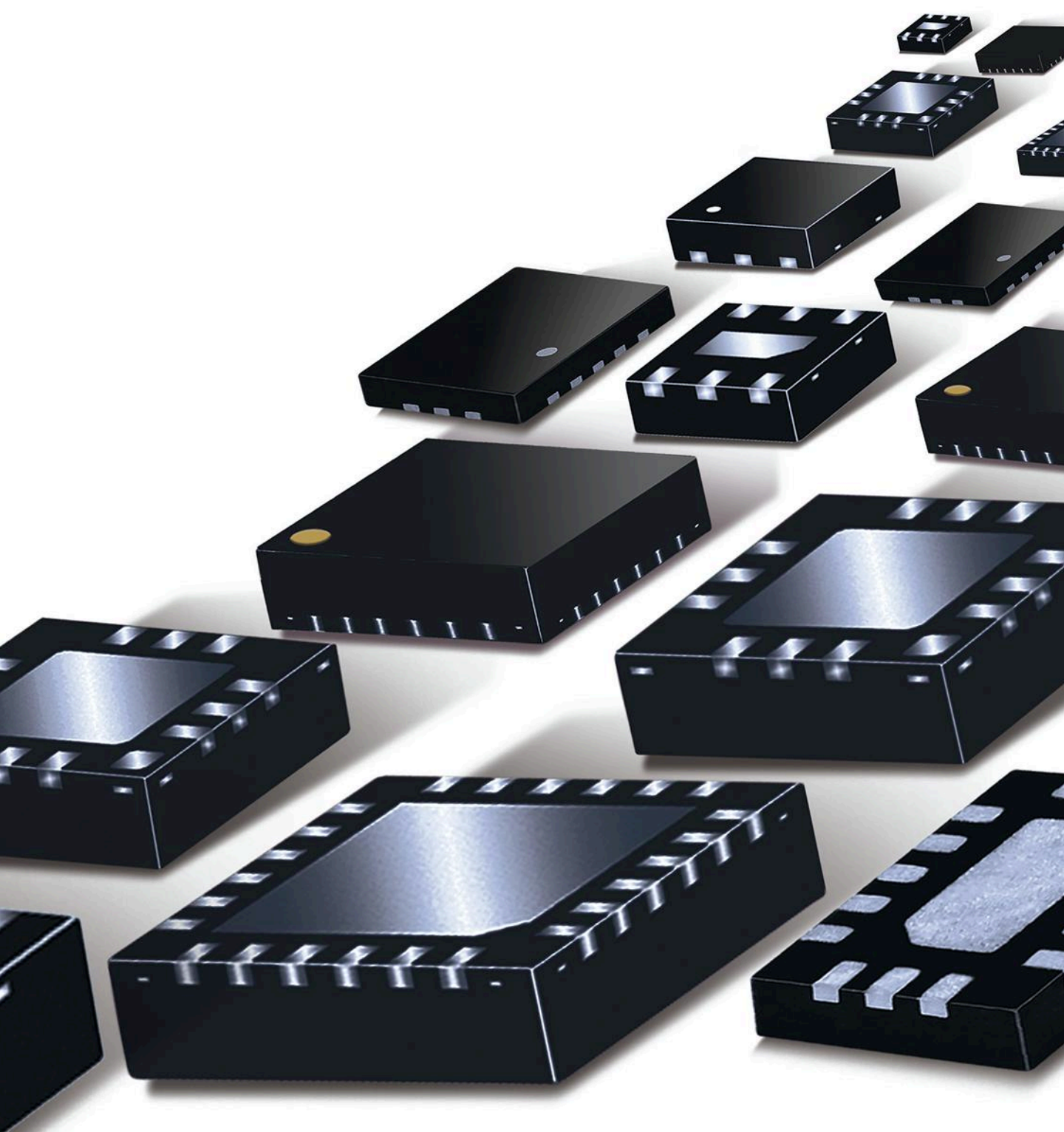
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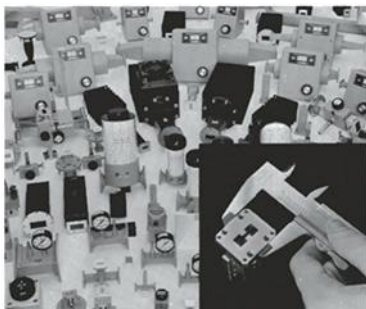
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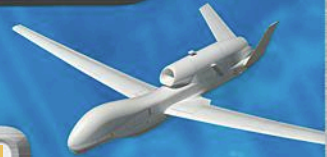


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OCTAVE BAND LOW NOISE AMPLIFIERS

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	3rd Order ICP	VSWR
CA01-2110	0.5-1.0	28	1.0 MAX, 0.7 TYP	+10 MIN	+20 dBm	2.0:1
CA12-2110	1.0-2.0	30	1.0 MAX, 0.7 TYP	+10 MIN	+20 dBm	2.0:1
CA24-2111	2.0-4.0	29	1.1 MAX, 0.95 TYP	+10 MIN	+20 dBm	2.0:1
CA48-2111	4.0-8.0	29	1.3 MAX, 1.0 TYP	+10 MIN	+20 dBm	2.0:1
CA812-3111	8.0-12.0	27	1.6 MAX, 1.4 TYP	+10 MIN	+20 dBm	2.0:1
CA1218-4111	12.0-18.0	25	1.9 MAX, 1.7 TYP	+10 MIN	+20 dBm	2.0:1
CA1826-2110	18.0-26.5	32	3.0 MAX, 2.5 TYP	+10 MIN	+20 dBm	2.0:1

NARROW BAND LOW NOISE AND MEDIUM POWER AMPLIFIERS

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	3rd Order ICP	VSWR
CA01-2111	0.4 - 0.5	28	0.6 MAX, 0.4 TYP	+10 MIN	+20 dBm	2.0:1
CA01-2113	0.8 - 1.0	28	0.6 MAX, 0.4 TYP	+10 MIN	+20 dBm	2.0:1
CA12-3117	1.2 - 1.6	25	0.6 MAX, 0.4 TYP	+10 MIN	+20 dBm	2.0:1
CA23-3111	2.2 - 2.4	30	0.6 MAX, 0.45 TYP	+10 MIN	+20 dBm	2.0:1
CA23-3116	2.7 - 2.9	29	0.7 MAX, 0.5 TYP	+10 MIN	+20 dBm	2.0:1
CA34-2110	3.7 - 4.2	28	1.0 MAX, 0.5 TYP	+10 MIN	+20 dBm	2.0:1
CA56-3110	5.4 - 5.9	40	1.0 MAX, 0.5 TYP	+10 MIN	+20 dBm	2.0:1
CA78-4110	7.25 - 7.75	32	1.2 MAX, 1.0 TYP	+10 MIN	+20 dBm	2.0:1
CA910-3110	9.0 - 10.6	25	1.4 MAX, 1.2 TYP	+10 MIN	+20 dBm	2.0:1
CA1315-3110	13.75 - 15.4	25	1.6 MAX, 1.4 TYP	+10 MIN	+20 dBm	2.0:1
CA12-3114	1.35 - 1.85	30	4.0 MAX, 3.0 TYP	+33 MIN	+41 dBm	2.0:1
CA34-6116	3.1 - 3.5	40	4.5 MAX, 3.5 TYP	+35 MIN	+43 dBm	2.0:1
CA56-5114	5.9 - 6.4	30	5.0 MAX, 4.0 TYP	+30 MIN	+40 dBm	2.0:1
CA812-6115	8.0 - 12.0	30	4.5 MAX, 3.5 TYP	+30 MIN	+40 dBm	2.0:1
CA812-6116	8.0 - 12.0	30	5.0 MAX, 4.0 TYP	+33 MIN	+41 dBm	2.0:1
CA1213-7110	12.2 - 13.25	28	6.0 MAX, 5.5 TYP	+33 MIN	+42 dBm	2.0:1
CA1415-7110	14.0 - 15.0	30	5.0 MAX, 4.0 TYP	+30 MIN	+40 dBm	2.0:1
CA1722-4110	17.0 - 22.0	25	3.5 MAX, 2.8 TYP	+21 MIN	+31 dBm	2.0:1

ULTRA-BROADBAND & MULTI-OCTAVE BAND AMPLIFIERS

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	3rd Order ICP	VSWR
CA0102-3111	0.1-2.0	28	1.6 Max, 1.2 TYP	+10 MIN	+20 dBm	2.0:1
CA0106-3111	0.1-6.0	28	1.9 Max, 1.5 TYP	+10 MIN	+20 dBm	2.0:1
CA0108-3110	0.1-8.0	26	2.2 Max, 1.8 TYP	+10 MIN	+20 dBm	2.0:1
CA0108-4112	0.1-8.0	32	3.0 MAX, 1.8 TYP	+22 MIN	+32 dBm	2.0:1
CA02-3112	0.5-2.0	36	4.5 MAX, 2.5 TYP	+30 MIN	+40 dBm	2.0:1
CA26-3110	2.0-6.0	26	2.0 MAX, 1.5 TYP	+10 MIN	+20 dBm	2.0:1
CA26-4114	2.0-6.0	22	5.0 MAX, 3.5 TYP	+30 MIN	+40 dBm	2.0:1
CA618-4112	6.0-18.0	25	5.0 MAX, 3.5 TYP	+23 MIN	+33 dBm	2.0:1
CA618-6114	6.0-18.0	35	5.0 MAX, 3.5 TYP	+30 MIN	+40 dBm	2.0:1
CA218-4116	2.0-18.0	30	3.5 MAX, 2.8 TYP	+10 MIN	+20 dBm	2.0:1
CA218-4110	2.0-18.0	30	5.0 MAX, 3.5 TYP	+20 MIN	+30 dBm	2.0:1
CA218-4112	2.0-18.0	29	5.0 MAX, 3.5 TYP	+24 MIN	+34 dBm	2.0:1

LIMITING AMPLIFIERS

Model No.	Freq (GHz)	Input Dynamic Range	Output Power Range Psat	Power Flatness dB	VSWR
CLA24-4001	2.0 - 4.0	-28 to +10 dBm	+7 to +11 dBm	+/- 1.5 MAX	2.0:1
CLA26-8001	2.0 - 6.0	-50 to +20 dBm	+14 to +18 dBm	+/- 1.5 MAX	2.0:1
CLA712-5001	7.0 - 12.4	-21 to +10 dBm	+14 to +19 dBm	+/- 1.5 MAX	2.0:1
CLA618-1201	6.0 - 18.0	-50 to +20 dBm	+14 to +19 dBm	+/- 1.5 MAX	2.0:1

AMPLIFIERS WITH INTEGRATED GAIN ATTENUATION

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure (dB)	Power-out @ P1-dB	Gain Attenuation Range	VSWR
CA001-2511A	0.025-0.150	21	5.0 MAX, 3.5 TYP	+12 MIN	30 dB MIN	2.0:1
CA05-3110A	0.5-5.5	23	2.5 MAX, 1.5 TYP	+18 MIN	20 dB MIN	2.0:1
CA56-3110A	5.85-6.425	28	2.5 MAX, 1.5 TYP	+16 MIN	22 dB MIN	1.8:1
CA612-4110A	6.0-12.0	24	2.5 MAX, 1.5 TYP	+12 MIN	15 dB MIN	1.9:1
CA1315-4110A	13.75-15.4	25	2.2 MAX, 1.6 TYP	+16 MIN	20 dB MIN	1.8:1
CA1518-4110A	15.0-18.0	30	3.0 MAX, 2.0 TYP	+18 MIN	20 dB MIN	1.85:1

LOW FREQUENCY AMPLIFIERS

Model No.	Freq (GHz)	Gain (dB) MIN	Noise Figure dB	Power-out @ P1-dB	3rd Order ICP	VSWR
CA001-2110	0.01-0.10	18	4.0 MAX, 2.2 TYP	+10 MIN	+20 dBm	2.0:1
CA001-2211	0.04-0.15	24	3.5 MAX, 2.2 TYP	+13 MIN	+23 dBm	2.0:1
CA001-2215	0.04-0.15	23	4.0 MAX, 2.2 TYP	+23 MIN	+33 dBm	2.0:1
CA001-3113	0.01-1.0	28	4.0 MAX, 2.8 TYP	+17 MIN	+27 dBm	2.0:1
CA002-3114	0.01-2.0	27	4.0 MAX, 2.8 TYP	+20 MIN	+30 dBm	2.0:1
CA003-3116	0.01-3.0	18	4.0 MAX, 2.8 TYP	+25 MIN	+35 dBm	2.0:1
CA004-3112	0.01-4.0	32	4.0 MAX, 2.8 TYP	+15 MIN	+25 dBm	2.0:1

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News

NEW DAC Aims to Ease System Design

Digital-to-analog converter (DAC) technology is one specialty of Teledyne e2v (www.teledyne-e2v.com), which has been developing such converter solutions for many years. The company recently announced its latest DAC, which it says can achieve clean signal generation at frequencies as high as 26.5 GHz.

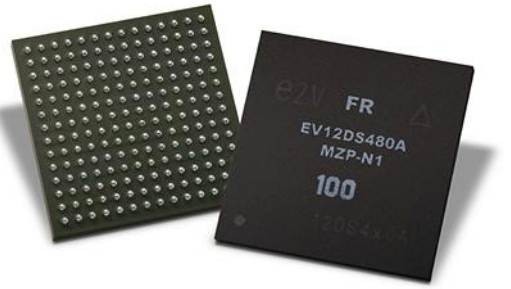
The recently unveiled DAC, the EV12DS480, is a 12-b DAC with a sampling rate of 8 Gsamples/s (see figure). Kurt Rentel, business development manager of signal processing solutions at Teledyne e2v, recently explained the new product in more detail.

“Teledyne has been developing really broadband data converters for a long time,” said Rentel. “On the D/A side, that means direct launching into some RF band. Original converters developed probably over 20 years ago were in the L-band range. Our new DAC has a sam-

pling rate of up to 8 Gsamples/s, and it also has 8 GHz of analog bandwidth.”

Rentel is quick to point out that the EV12DS480 is still usable beyond 8 GHz. “It rolls off after 8 GHz—but it’s a single pole roll-off and it’s got a $\sin(x)/x$ roll-off as well,” he explained. “That allows our customers to actually use it above its 3-dB bandwidth. It’s being used at 10 GHz; some people are considering it at X-band; some people are looking at using it up into Ku- and Ka-band because it still has reasonable power and it really simplifies systems—you have digital bits going in one end and RF out the other.”

According to Rentel, system simplification is a major advantage that the EV12DS480 brings to the table. “The simplified-system aspect of this is that you get rid of analog upconversion stages with the DAC. If you look at a block diagram, the EV12DS480 takes a chunk



The EV12DS480 achieves a sampling rate of 8 Gsamples/s and can be used in systems that operate all the way into Ka-band frequencies.

away from it. This DAC takes away a mixer and a synthesizer that had to drive that mixer and replaces them with their digital equivalents. That happens in a FPGA or some type of processing unit that sits in front of the DAC.”

So what applications are being targeted? “As a business unit, we focus a lot on high-reliability, high-performance, long-life systems,” added Rentel. “Avionics and space applications fall into that category. This product is designed and specified to be used in high-reliability applications like aircraft systems and space. If you want long life and very reliable operation, you need to have high-reliability components. We start by saying that we want these products to work for these high-reliability applications—and then we will certainly move into less stringent areas like instrumentation and some of the communications systems.” ■

GROUND STATIONS Provide Enhanced Control of GPSIII Satellites

IN SUPPORT OF the launch of the first, next-generation GPS III satellite (GPS III SV01) by Lockheed Martin, Raytheon Co. (www.raytheon.com) has developed the GPS Next-Generation Control System (GPS OCX) for maneuvering and controlling the orbiting satellite. Achieving the final, precise orbit for this timing/position-location satellite is a painstaking operation that requires 10 or more days to accomplish using the GPS OCX.

“The GPS OCX Block 0 launch and checkout system is foundational to the

improved precision, navigation and timing of the entire constellation,” said Dave Wajsglas, president of Raytheon Intelligence, Information, and Services, “and we’ll all benefit from the system’s unprecedented level of cybersecurity protections.”

This latest generation of the GPS OCX station will also support the launch of future GPS III satellites to enhance GPS timekeeping/positioning capabilities and GPS accuracy for both military and civilian users. It will also handle more than

twice the GPS satellites as earlier ground control systems. The ground system features an open architecture that allows upgrades when needed and integration of new capabilities when required. However, it also provides the highest level of cybersecurity protection claimed for any U.S. Department of Defense (DoD) space system to guard against cyberthreats.

The open architecture permits modifications at any time in response to new cyberthreats. Delivery of the GPS OCX ground stations will take in stages or



Harold Brown, who had an illustrious career leading the development of advanced technology in the U.S. military, and who served as Secretary of Defense under President Jimmy Carter, passed away on Jan. 4 at age 91. (Courtesy: The Scotsman)

Industry, Armed Forces Remember **HAROLD BROWN**

HAROLD BROWN, the 14th Secretary of Defense for the U.S. Department of Defense (DoD), passed away at his home in Rancho Sante Fe, Calif., last month; he was 91. Brown was the first scientist to serve as Secretary of Defense for the U.S. Armed Forces. He served in the role from 1977 to 1981 under President Jimmy Carter after previous stints as U.S. Air Force Secretary under President Lyndon B. Johnson during the Vietnam War and Director of U.S. Defense Research and Engineering under President John F. Kennedy.

Brown was a proponent of achieving national security using advanced technology and strong arms control. He supported

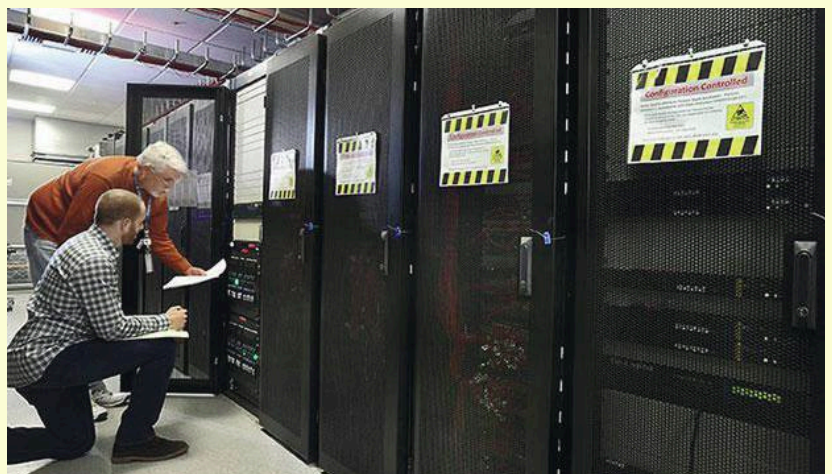
deterrence through a buildup of nuclear weapons and capabilities and encouraged the development of air-launched missiles, such as the Peacekeeper missile.

The acting Secretary of Defense, Patrick M. Shanahan, praised Brown's life and contributions: "Dr. Brown led a remarkable life, first as an academic and scientist, and then as a public servant in a variety of prominent roles. He shaped our nation's military for more than two decades, revolutionizing the development of naval munitions, renovating America's post-Vietnam War weapons platforms, developing stealth aircraft, and leading nuclear weapons research." ■

blocks, beginning with the delivering of the Block 0 GPS OCX station to enable the launch and positioning of the first GPS III satellite. Additional deliveries, as Block 1 and Block 2 GPS OCX systems, are planned for delivery by 2021. These will increase ground control capabilities for additional GPS III satellites in the GPS constellation. ■

The GPS OCX Block 0 launch and checkout system for controlling GPS III satellites was installed at Schriever Air Force Base.

(Courtesy: Raytheon Co.)



SPACE COMMAND Will Integrate Military Capabilities

SPACE HAS OFTEN been called “the final frontier.” During a visit late last year by Vice President Mike Pence to the Kennedy Space Center in Florida, he referred to the U.S. Space Command as a critical portion of this country’s

armed forces. Prior to the launch of the Vespucci third-generation GPS (GPS III) satellite, during a Dec. 18 visit to the Florida facility, Pence referred to Space Command as a work in progress that will integrate many different military space

capabilities from all branches of the military. “It will serve alongside other functional commands like Strategic Command and Special Operations Command, and it will be led by a four-star flag officer,” he said. “It will establish unified control over all our military space operations.”

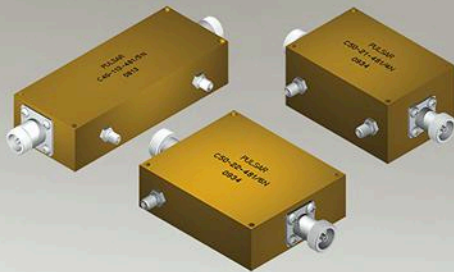
Pence called the U.S. Space Command the U.S. military’s 11th unified combatant command. “It will develop the space doctrine, tactics, techniques, and procedures that will enable our warfighters to defend our nation in this new era,” he noted. It would become the sixth branch of the armed forces in the future, with the current (Trump) administration working with Congress to establish a working U.S. Space Force before the end of 2020. ■



Vice President Mike Pence was joined by U.S. Air Force Secretary Heather Wilson at Florida’s Kennedy Space Center this past December prior to the launch of the first GPS III satellite, marking the beginning of space-based armed forces. (Courtesy: U.S. Department of Defense)

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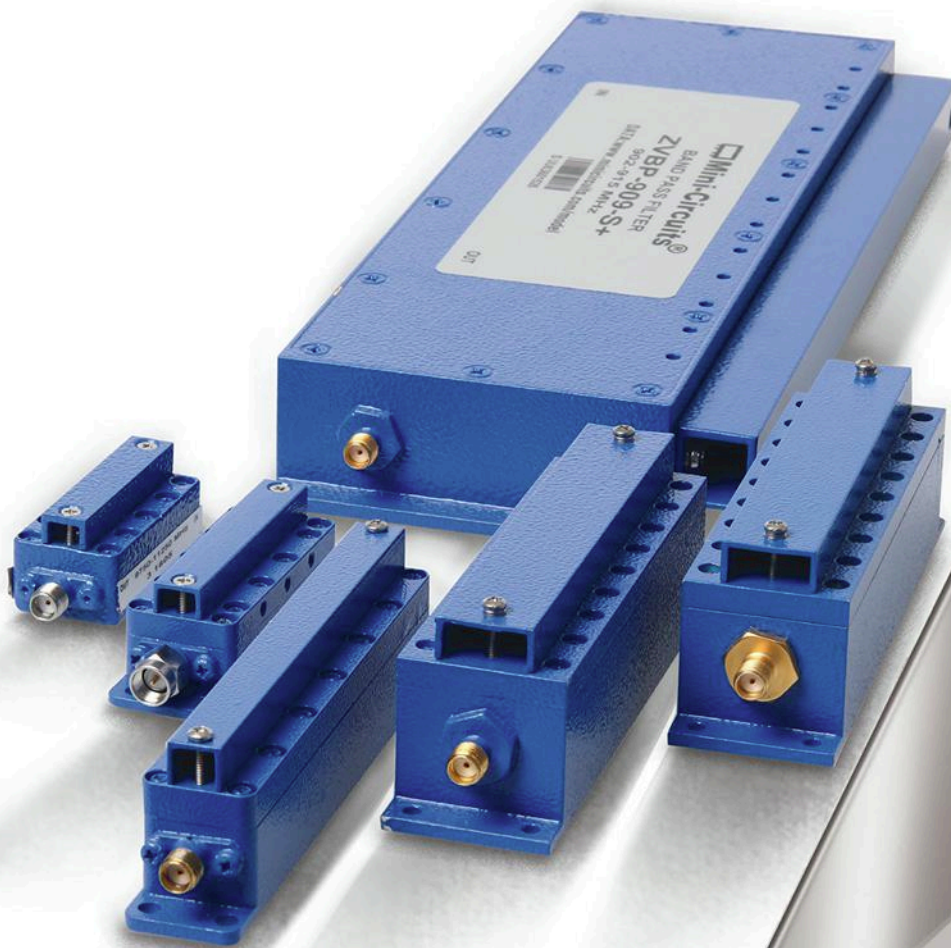
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0.5-50	50 ± 1	0.10	0.50	20	2000	C50-100
0.5-100	30 ± 1	0.30	0.50	25	200	C30-102
0.5-100	40 ± 1	0.20	0.30	20	200	C40-103
1.0-100	50 ± 1	0.20	1.00	20	500	C50-109
20.0-200	50 ± 1	0.20	0.75	20	500	C50-108
0.1-250	40 ± 1	0.40	0.50	20	250	C40-111
50-500	40 ± 1	0.20	1.00	20	500	C40-21
50-500	50 ± 1	0.20	1.00	20	500	C50-21
100-1000	40 ± 1	0.40	1.00	20	500	C40-20
500-1000	50 ± 1	0.20	0.50	20	500	C50-106
80-1000	40 ± 1	0.30	1.00	20	1000	C40-27
80-1000	50 ± 1	0.30	1.00	20	1000	C50-27
80-1000	40 ± 1	0.30	1.00	20	1500	C40-31
80-1000	50 ± 1	0.30	1.00	20	1500	C50-31

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News

STARTUP'S ENERGY-HARVESTING CHIPS Run on Radio Frequencies



WILIOT, A STARTUP developing Bluetooth chips that can be powered by ambient radio frequencies, has raised \$30 million in funding from Qualcomm Ventures, Samsung Venture Investment, Avery Dennison, and Amazon Web Services, among others. The funding increases the company's total to \$50 million as it moves closer to entering production.

The chips can be slapped on tags as small as a fingernail, as thin as a sheet of paper, and that incorporate sensors. According to Wiliot, the devices can broadcast data such as location, weight, and temperature over Bluetooth. Wiliot's technology lets them communicate with smartphones or other Bluetooth devices using energy harvested from Wi-Fi, cellular and Bluetooth—no batteries required.

The sensors can be used in all sort of devices unconnected to the Internet of Things, ranging from spare parts in a manufacturing plant to the packaging around consumer goods. The sensors could be pasted on products during production to track them from the factory to the warehouse to the store. They could also replace clothing tags, giving customers the ability to scan for more details.

"Wiliot's strategy for battery-free Bluetooth transponders, which sense and communicate without needing specific action by consumers, is very relevant to Avery Dennison's intelligent label strategy," Francisco Melo, general manager of Avery Dennison's radio-frequency iden-

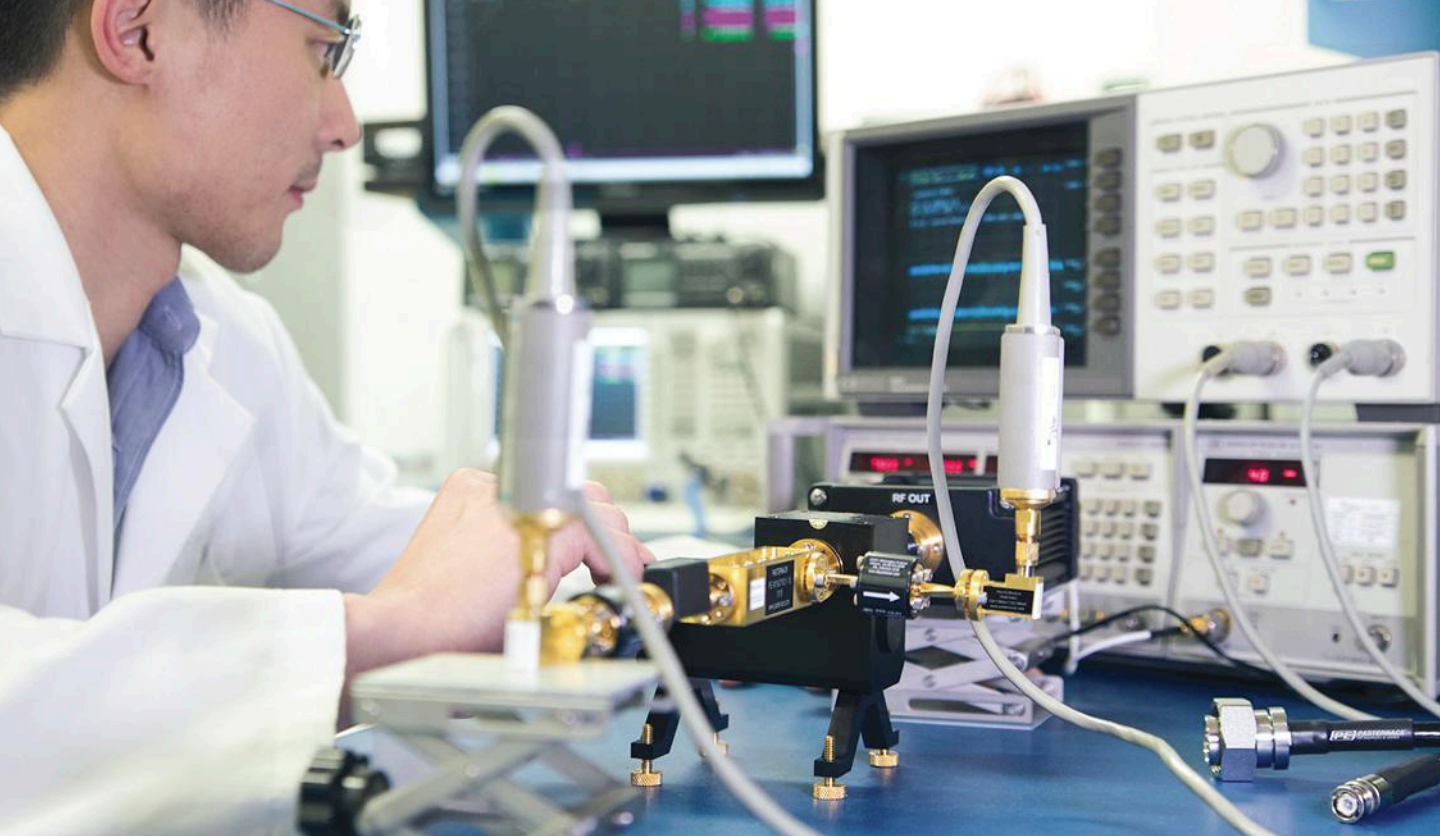
tification (RFID) unit, said in a statement. Avery Dennison is one of the largest RFID manufacturers in the world.

Wiliot, which has around 40 employees and is based in San Diego, Calif., is the second company founded by the team behind semiconductor startup Wilocity. The company raised roughly \$100 million in investment to build chips based on the next-generation Wi-Fi standard—more commonly called WiGig—targeting the personal-computer and peripherals markets. Qualcomm bought it for around \$400 million in 2014.

"We believe that disposable electronics based on battery-free, low-cost systems are the foundation for future Internet of Things systems," chief executive and founder Ta Tarim said. "Recycling the radiation around us to power sticker-size sensors can enable new ways for consumers to interact with products that were previously not feasible," added Tarim, a former vice president of product management at Qualcomm.

Other companies are operating in the energy-harvesting chip market. Atmosic Technologies, which was founded by former engineering executives at Qualcomm Atheros, is building Bluetooth chips for consumer electronics such as wearables that are capable of running on radio frequencies directed at them from other Bluetooth devices. The company's chips are not dependent on ambient energy like those from Wiliot. ■

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MICROWAVE ABLATION Helps Attack Tumors

MICROWAVE ENERGY is well known for its heating effects at certain frequencies/wavelengths. One of the keys for using microwave ablation (MWA) for medicinal reasons, specifically to heat and destroy cancerous tumors in patients, is finding the optimum antenna for each case. With the wrong antenna and coaxial feed lines, healthy tissues can be heated (and overheated) along with the cancerous tissues, causing unwanted damage to those tissues. To complicate matters, when using minimally invasive interstitial antennas to apply microwave energy to cancerous tumors, the antenna's input impedance depends on the insertion depth.

Among the antennas designed for MWA treatments, a triaxial antenna employs a biopsy needle in a floating sleeve over the outer conductor. For a given insertion depth, the position of the needle is adjusted to create the best impedance match for the antenna. Another design, a balun-free antenna, operates at the second resonant frequency of a monopole to achieve a given specific-absorption-rate (SAR) pattern and ablation zone for the applied microwave energy without using a coaxial balun. Yet another antenna configuration, a choke antenna, uses short-circuited quarter-wavelength sleeves as part of the MWA process.

In the interest of finding an optimum antenna configuration for MWA on humans, researchers from the University of Wisconsin-Madison performed experiments with the different antennas on ex vivo bovine livers to examine the ablation zones obtained from each antenna. The bovine livers were exposed to microwave radiation at a power level of 40 W for a

total of 5 min. for each antenna. Test signals were produced by boosting the outputs of a commercial microwave signal generator through a solid-state power amplifier and then feeding each antenna.

After each five-minute application of microwave energy at 1.9 GHz, the bovine liver was cut along the insertion path of the antenna and the ablation zone of each antenna was measured. Each antenna's ablation zone was ellipsoidal in shape. By means of visual inspection and careful measurements, the aspect ratio of each ablation zone was ascertained to determine the most spherical of the ablation zones for the three antennas, since many tumors are spherical in shape.

The experiments revealed that the choke dipole antenna and the balun-free base-fed monopole antenna produced the most spherically shaped ablation zones of the three types of MWA antennas, with the triaxial antenna providing the least spherical of the ablation zones. The triaxial and choke antennas are both currently used in FDA-approved commercial MWA systems.

Electromagnetic (EM) computer software simulations showed that each of the antennas could provide a good impedance match with the bovine liver at the desired operating frequency. However, the choke and balun-free antennas provided the most compact and localized power absorption patterns, with much less extra heating of surrounding tissues compared to the triaxial antenna.

See "Tools for Attacking Tumors," *IEEE Antennas & Propagation Magazine*, Vol. 60, No. 6, December 2018, pp. 52-57.

U-SHAPED WAVEGUIDE Paves Way to THz ICs

OVERCROWDING OF SIGNALS at RF and microwave frequencies has created growing interest in millimeter-wave and even terahertz (THz) frequency bands for short-range applications. In turn, circuit designers are exploring ways to integrate different components and transmission lines at higher frequencies.

One of the transmission-line approaches for THz frequencies consists of a U-shaped silicon (Si) guiding channel attached to a glass substrate, such as Pyrex glass—a structure known as U-shaped silicon-on-glass (U-SOG). The Si guiding channel is etched from below the guiding channel to reduce interaction of the modal fields with the Pyrex substrate material, resulting in a low attenuation constant for the waveguide structure.

Nazy Ranjesh and fellow researchers from the University of Waterloo (Ontario, Canada) designed a U-SOG waveguide structure with the aid of High Frequency Structure Simulator (HFSS) modeling software from Keysight Technologies along

with the same company's PNA-X vector network analyzers (VNAs) and a specially designed test fixture. The attenuation constants for the U-SOG waveguide structure compare closely between simulated and measured values, with low attenuation from 800 GHz through 1.1 THz.

Simulated values are usually less than the measurements, due to the difficulty of achieving proper alignments between the U-SOG structure and the standard metallic waveguide test fixtures. But compared with other transmission-line technologies, including metallic waveguide, the U-SOG approach does quite well in preserving signal power even at these high frequencies, making it a good candidate for on-chip transmission lines and integrated circuits at THz frequencies.

See "1.1 THz U-Silicon-On-Glass (U-SOG) Waveguide: A Low-Loss Platform for THz High-Density Integrated Circuits," *IEEE Transactions on Terahertz Science and Technology*, Vol. 8, No. 6, November 2018, pp. 702-709.

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Employ Design-Flow Integration for Advanced Multichip RF Design

A new workflow allows designers to combine multiple technologies that originate from different software tools into a single project.

Evolving communication standards like LTE-A and 5G are driving future RF architectures and, consequently, creating challenges for RF front-end module design in terms of miniaturization, performance, and support for technologies that boost data throughputs by improving spectral efficiency.

To meet the ongoing need for higher performance and reduced component size in multimode- and multiband-capable handsets, companies are shifting their module integration strategies from combining similar building blocks in a single package to adopting multifunctional front ends based on diverse technologies. These development efforts target products based on a single, fully integrated RF module for each frequency range, including multimode/multiband power amplifiers (PAs), duplexers, RF switches, and RF matching.

Module and subsystem designers often use more than one technology in a complete design. These technologies include gallium-arsenide (GaAs) and gallium-nitride (GaN) monolithic microwave integrated circuits (MMICs), silicon (Si) RF integrated circuits (RFICs), and multiple-layer laminates. Each technology is encapsulated in a specific process design kit (PDK)

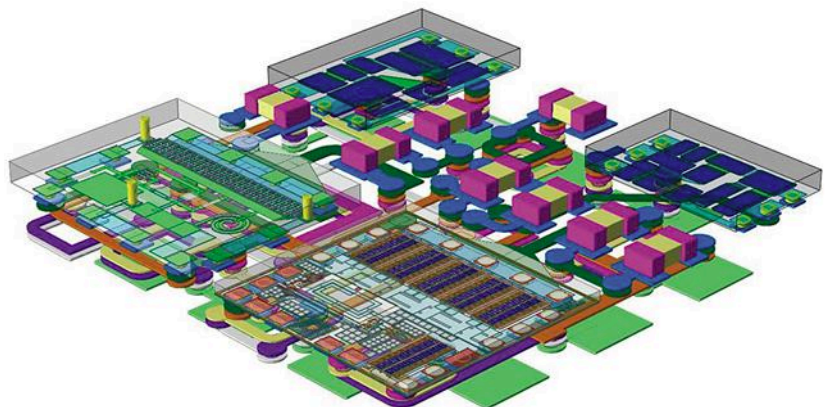
that details the electrical and physical attributes of the manufacturing process and front-end building blocks (component libraries).

A multi-technology design flow that supports multiple PDKs and circuit/electromagnetic (EM) co-simulation is used to analyze the electrical interactions between the bulk-acoustic-wave (BAW) and surface-acoustic-wave (SAW) filters (based on equivalent circuit models) and multi-layer laminate package. It provides comprehensive module analysis and optimization. However, the Si RFIC switch, low-noise amplifier (LNA), and PA development is often executed in Cadence (www.cadence.com) software using a Cadence Si PDK.

This article presents a modern design flow that translates the Cadence PDK into one that can be simulated in the NI AWR Design Environment platform to support chip-package co-design and EM verification. By importing the design into a dynamic library that can be used alongside the Cadence PDK, designers are able to effectively develop products based on disparate technologies using complex designs originally created in completely different environments.

EDA TOOLS ARE BUILT FOR SPECIFIC NEEDS

Designers use different RF electronic-design-automation (EDA) tools based on personal preference and the capabilities of a particular tool to address a



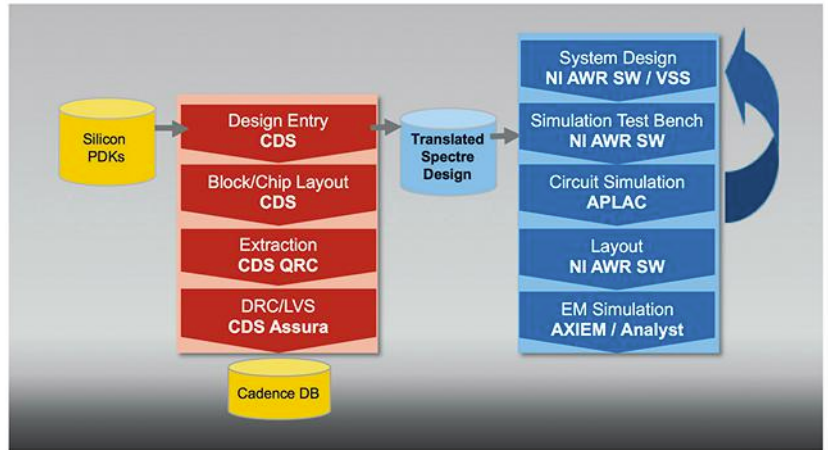
1. Shown is a typical module design in the Microwave Office software.

single or set of design tasks. Some tools specialize in high-frequency MMIC, printed-circuit-board (PCB), and module design, such as Microwave Office circuit design software. Others like Cadence target silicon-based RFIC and module design. Since each of these tools have their own individual strengths, it's best to adopt those that support interoperability and the exchange of information in a well-defined design flow so that designers can take advantage of the best tool for each design task.

To support data exchange between different environments, several industry-standard file formats have been developed, such as touchstone (SNP) and measurement data interchange format (MDIF) files. The touchstone file provides S-parameters, the small-signal simulated or measured frequency response of a network. An MDIF file allows data such as S-parameters or noise to be sorted by an unlimited number of independent variables like frequency or gate voltage. These formats allow designers to model the linear response of devices (e.g., an RFIC or a switch) in their simulation and easily bring that model back and forth between design tools.

Polyharmonic models, sometimes referred to as Keysight X-parameters, are analogous to S-parameters, with the added capability to simulate nonlinear behavior resulting from large-signal operating conditions. Other data formats used between different design tools include Spice netlists for circuit blocks, interchange file format (IFF) for schematic information, and layout formats like GDSII and DXF.

These standard formats can work adequately, but they each have their limitations. For instance, S-parameters are for linear simulation—they do not work for nonlinear simulations. And some RF simulators can only use two-port MDIF files. Large-signal polyharmonic models can take a long time to generate and simulate, and the files tend to be quite large, making them hard to share. Specifically,



2. This diagram illustrates the Cadence Spectre translation flow for co-simulation in the NI AWR Design Environment platform.

for X-parameters, the files can be in the gigabytes.

DESIGN CHALLENGES FOR MODULE AND SUBSYSTEM DESIGNERS

For RF modules that integrate multiple technologies developed with a range of tools, the need for greater interoperability between tools often goes beyond simple data-format compatibility due to the complexity of the overall design task. Front-end modules and other multi-technology devices can contain upwards of 25 integrated circuits (ICs) on a single laminate module, including BAW and SAW filters, III-V RF MMIC PAs, silicon switches with multiple antennas, and silicon LNAs. In this article's design example, the silicon switches and LNAs were designed in Cadence and the acoustic/laminate filters were done in the Microwave Office software. *Figure 1* shows what a typical multichip module design would look like.

A less-automated design flow would incorporate the performance of the RFICs modeled in Cadence Virtuoso using small-signal touchstone S-parameters, with one file for each switch state, or an MDIF with the switch state represented by a parameterized variable. Either approach requires large files

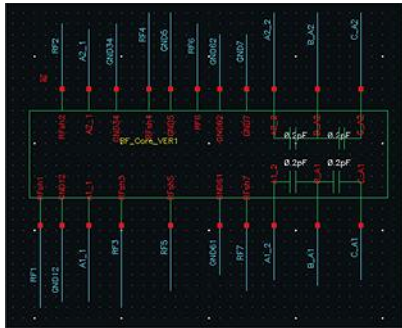
that must be created, updated with any design changes, and then shared across design teams.

Creating the necessary files for all the needed switch states is time-consuming for the switch designer. The process could be error-prone in support of the more than 250 states covered by the RFIC. In the case of the touchstone files, only linear behavior is captured. The nonlinear behavior, which is critical to switches and even acoustic filters, would need to be captured by the larger polyharmonic file. With the RFIC analysis and S-parameter file generation taking seven minutes per state with 68 states for one switch and 25 states for the other, a huge time investment is required—one that would take hours or even days to generate.

CADENCE VIRTUOSO AND NI AWR SOFTWARE CO-SIMULATION FLOW

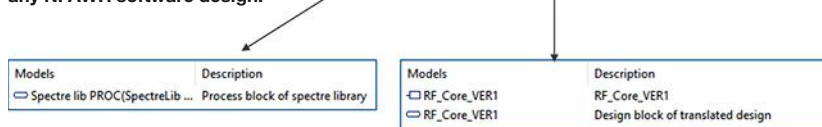
The solution featured in this article utilized new capabilities that support Cadence designs directly within the Microwave Office software. *Figure 2* shows an overview of this flow. Here, a design flow based on the translation of the Cadence Spectre netlist within Microwave Office circuit simulation enables Cadence Virtuoso and NI AWR software co-simulation.

The flow is made possible by taking the silicon process PDK in Cadence and translating both the PDK and design and transporting them via a Spectre design netlist into the Microwave Office software, where the designer has access to all NI AWR Design Environment tools. These tools include Visual System Simulator (VSS) system design

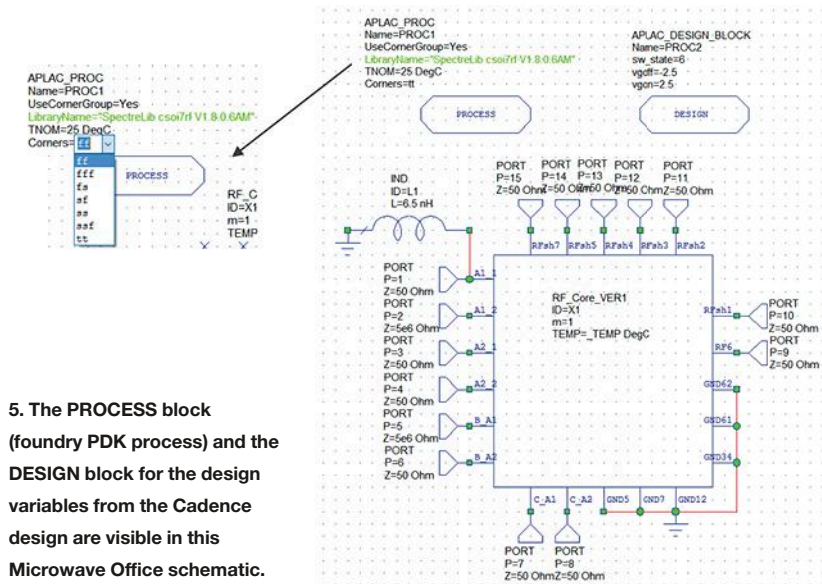


3. This is a Cadence Virtuoso switch schematic.

4. The translated Cadence foundry PDK (left) and the design PDK (right) appear in the element tree library, ready for insertion in any NI AWR software design.



5. The PROCESS block (foundry PDK process) and the DESIGN block for the design variables from the Cadence design are visible in this Microwave Office schematic.



software, Microwave Office linear and nonlinear simulation, APLAC harmonic balance and transient simulation, NI AWR layout tools, and AXIEM 3D planar and Analyst 3D finite-element method (FEM) EM simulators.

Figure 3 reveals the Cadence Virtuoso schematic for a double-pole/eight-throw (DP8T) silicon switch with on-die filter. The critical component is the antenna switch module (ASM), which has six different switch states.

NETLIST AND RUN

Using the “Netlist and Run” command within Cadence will create the files needed for NI AWR software translation. Since this command is run from a test-bench level, the schematic that must be translated is actually a subcircuit. The most critical file created is

input.scs, which contains all of the relevant Cadence schematic information.

Running the “Import Spectre Netlist Design” script will bring up a simple user interface dialog. Translation of this switch design (approximate 2,000-line netlist) took roughly one second. When the translation is complete, two components are available for use in any design: one for the process and the other for the actual design.

A log file is also generated that provides the designer and/or design support team with more detailed information concerning the cells that were translated, the libraries used, and the test-bench simulations. The translation includes microstrip-line (MLIN) elements from the original design, which provides accurate modeling of dispersion and loss in the transmission lines found within the design. In addition, directory paths to any files containing S-parameter blocks on the Cadence side are captured.

Once the switch design is translated, the user loads the two new PDKs into a new or existing project in Microwave Office software: the translated Cadence foundry PDK (cso7rf global foundries PDK; Fig. 4, left) and the design PDK (RF-Core; Fig. 4, right). The RF Core file provides both the schematic element and the design block. These PDKs will provide three simple NI AWR software library elements needed for simulation.

The new library elements are available through standard “drag and drop” placement into a Microwave Office circuit design software schematic, just like any other schematic element. Looking at the schematic view in Figure 5, the PROCESS block is used to reference the foundry PDK process and allows the user to alter the process corners. With the DESIGN block, the user can access any design variables within the Cadence design.

It can be seen on the right that this translated component has roughly 20 ports. The DESIGN block is where the switch state is controlled (set to 6 in this



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example), as well as the two voltages that will control the switch state. The PROCESS block on the top left (highlighted on the left side of the figure) provides designers with the ability to specify the process corners, which is very important for developing silicon IC designs.

To verify the frequency response of the netlist translation simulated in Microwave Office versus the original Spectre results, the S-parameters from a test-case Spectre simulation were imported into Microwave Office for comparison. The verification setup is virtually identical to the schematic test bench containing the translated netlist. For this simulation, the subcircuit contains the touchstone S-parameter block exported directly out of Cadence.

COMPARING SMALL-SIGNAL RESULTS

Figure 6 shows a comparison of the small-signal response (insertion loss) through a single path for the NI AWR software simulation of the translated netlist versus the Spectre results. This is represented by S-parameters across the entire frequency band. As expected, the results show exact agreement between the two results.

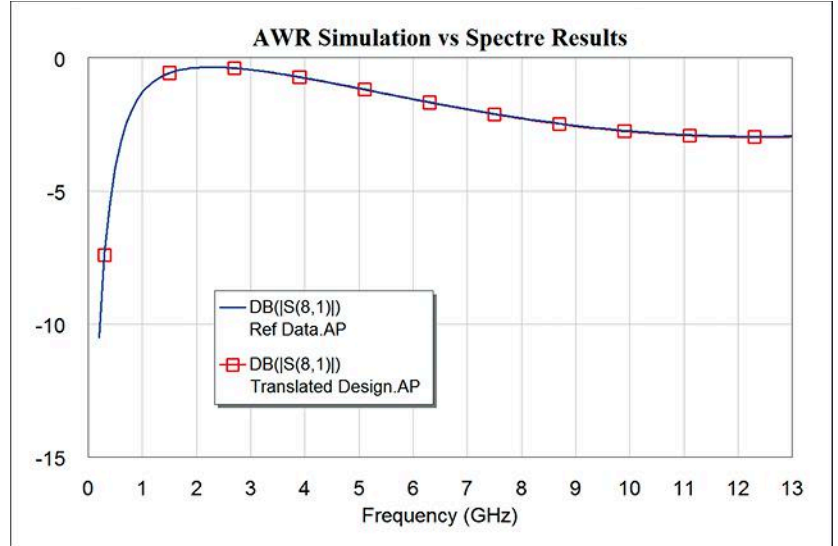
ADDITIONAL ANALYSIS

Now that the design translation has been verified, many other simulations can be performed with the switch, which includes sweeping the process corners, tuning/sweeping the switch state, and tuning/sweeping the control voltages. The imported RFIC behaves just like a regular Microwave Office element. On the left side of Figure 7, the swept process corners have been compared to reference data taken directly from Cadence, showing the impact of the process corners and the overlap between simulators.

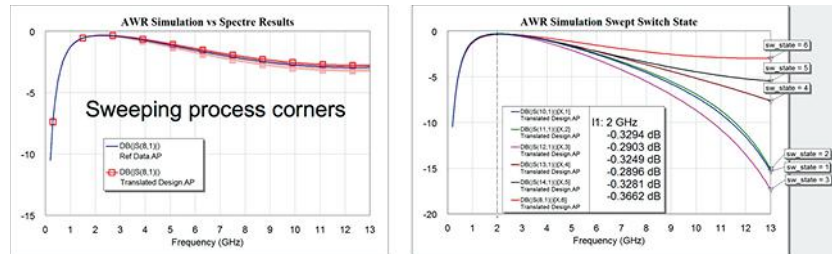
The right side of Fig. 7 reveals the simulated insertion loss for different switch states (through paths) in this example. The RFIC has been controlled through six different switch states. The differ-

ent responses, depending on the switch state, are shown. The designer can now develop the laminate design details based on an accurate RFIC model easily changing states through parameter settings, which can be tuned or swept.

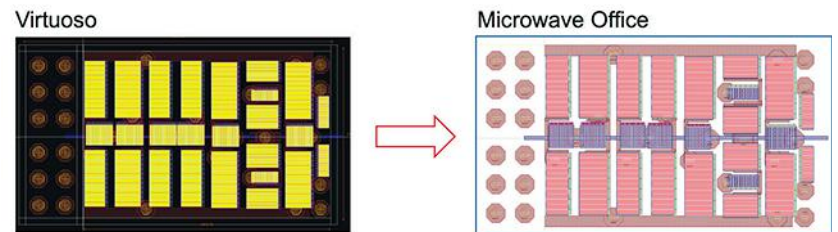
Furthermore, as the switch design is now a regular Microwave Office sub-circuit, it can be combined with any other Microwave Office elements, EM structures, data files, and more. It's possible to combine multiple technologies



6. The small-signal results from the NI AWR software simulation are compared with the Spectre results.



7. Other simulations can now be run with the switch because it behaves like a regular Microwave Office element.



8. The switch layout is able to be exported out of Cadence Virtuoso and imported into NI AWR software, where it can then be associated or linked with the schematic subcircuit to ensure proper layout connectivity.

into a single Microwave Office project, enabling co-simulation across technologies, as well as layout integration. A single laminate module can contain and combine Si switches, III-V PA RFICs, acoustic filters, and more. The final integrated design layout includes acoustic filters along with Si-device, GaAs-PA, and module technology.

It's possible to combine multiple technologies into a single Microwave Office project, enabling co-simulation across technologies, as well as layout integration. A single laminate module can contain and combine Si switches, III-V PA RFICs, acoustic filters, and more. The final integrated design layout includes acoustic filters along with Si-device, GaAs-PA, and module technology.

ASSIGNING LAYOUT

The switch layout can also be exported out of Cadence Virtuoso in a standard format like GDSII and imported into NI AWR software, where it can then be associated or linked with the schematic subcircuit to ensure proper layout connectivity (Fig. 8). The layout geometries are identical, with the colors being different simply as a matter of preference.

CONCLUSION

This article presented an integrated design flow for combining multiple

technologies originating from different software tools into a single project, enabling co-simulation across simulation and layout design tools. This flow allows designers to not only integrate different semiconductor and packaging (laminate) technologies, but leverage complex designs that were originally

created in a leading RFIC design environment for incorporation into a design environment specialized for MMIC, RF PCB, and module development. The final integrated design layout includes four different technologies: acoustic filters, a silicon device, a GaAs PA, and module technology. **MW**

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Striking the Right Balance: RF Power Output and Efficiency

Optimizing the cost and operating time for portable electronic systems running on batteries often comes down to one critical system-level parameter: efficiency.

Efficiency in electronics is a measure of how well a device or system does with the power available to it. For a battery-powered product, it's easy to tell when it's efficient, since more efficient products will operate for longer time periods on a given battery charge. With the world moving to portable cell phones and eventually 5G cellular systems, cellular radios with high efficiency will contribute to effective wireless communications networks and longer talk times per charge. High efficiency isn't confined to just power amplifiers (PAs) within the system, though; it involves all of the components that contribute to minimizing signal losses and power.

Efficiency in an RF/microwave system can be described in its simplest form as the amount of RF/microwave output power that's produced, such as from a PA, from a given amount of dc input power, such as a power supply or a battery. Although the concept is simple, efficiency may not be easy to determine for an application. That's because it depends on the type of active device or devices used in a PA, the operating frequency, temperature, the drive level, and even the impedance of the load. Even comparing a transmitter based on

an electron-tube configuration, such as a traveling-wave tube (TWT), to a solid-state PA based on the latest gallium-nitride (GaN) power transistors will provide some insight into how efficiency can differ drastically for the same frequency range and output power level.

Achieving high efficiency in an electronic system is a common goal for designers, although it can be quite challenging and may involve many components in the system. Power efficiency is usually associated with an electronic system's active components, such as the PAs in a radio's transmitters and low-noise amplifiers (LNAs) in a receiver.

A receiver and its LNAs are always typically powered on and the transmitter and PA are powered on only when signals are being sent to another receiver. It's the efficiency of the PA, though, that can have the greatest impact on the overall efficiency of a transmit/receive system.

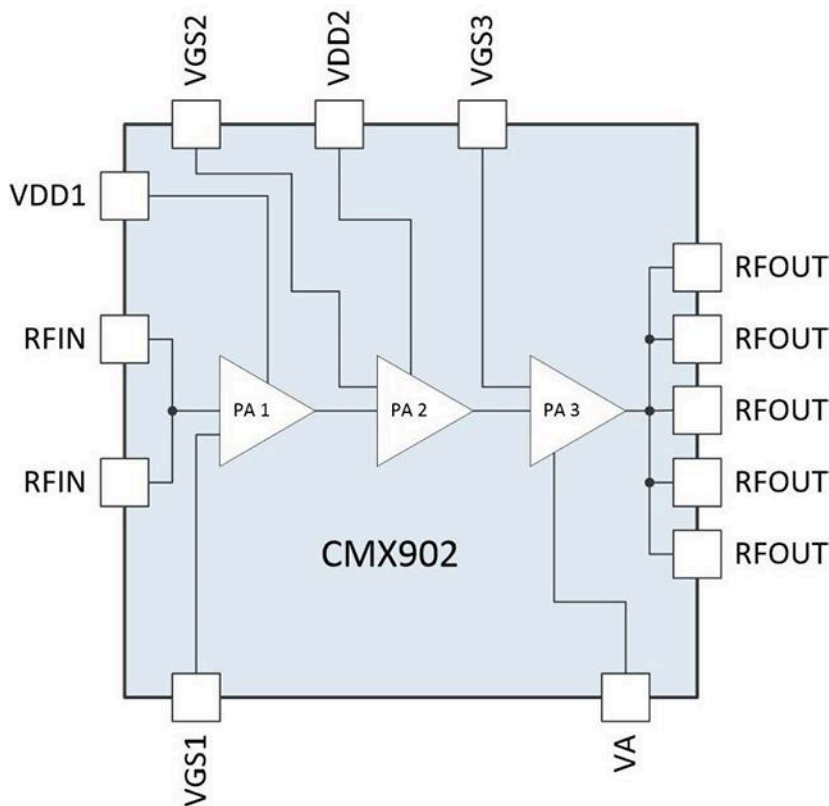
Still, a system's passive components can also contribute to efficiency. Energy is often dissipated as heat by way of some form of loss. For example, the insertion loss of the input and output coaxial cables and connectors can lower the efficiency of the PA by turning some of its power into heat. Especially for

applications that rely on batteries, high efficiency is an important performance parameter and can make a significant difference in an electronic system's useful operating time.

Efficiency can pertain to many different components within a system, including the semiconductor devices within its PAs. Device-level efficiency refers to the ratio of power applied to the input of the device (dc voltage and current) and the RF/microwave power generated at the output of the device. For a bipolar transistor, dc power is applied to the device collector and the device efficiency is called collector efficiency. For a field-effect transistor (FET) or high-electron-mobility transistor (HEMT), the dc power is fed to the device drain, so in this case, device efficiency is called the drain efficiency.

CLASSIFYING AMPLIFIERS

Estimating the efficiency of a high-frequency circuit or system usually starts with its choice of active components, notably amplifiers. A choice of RF/microwave amplifier is usually a compromise between linearity and efficiency, as denoted by the number of different amplifier architectures, such as Classes A, B, AB, C, D, E, F, G, and H.



1. Model CMX902 is a three-stage RF PA that combines Class A, Class AB, and Class C stages for good linearity and high efficiency at the same time, all in a 5- x 5-mm package. (Courtesy of CML Microcircuits)

Class A amplifiers, for example, provide very good linearity, but usually with fairly low efficiency compared to the other amplifier architectures. In practical commercial designs, such as the model CMX902 PA from CML Microcircuits (www.cmlmicro.com), multiple stages using different amplifier classes may be integrated to combine good linearity with high efficiency (Fig. 1).

Class A amplifier stages (Fig. 2) are implemented with a single active device, such as an electron tube or transistor, and are often referred to as “single-ended” amplifiers for that reason. They provide low distortion and good linearity for input signal waveforms by supplying bias power and the active device’s conduction at all times. The bias energy (voltage and current) may be varied in response to changes in the input signal waveform, but the power is always on,

with the best efficiency usually being 50% or less. For amplifiers, one form of efficiency that considers the amount of power in the input signal waveform is known as the power-added efficiency (PAE).

When the efficiency of an RF/microwave amplifier considers the effects of the amplifier’s gain on the difference between the output power and input power of the amplifier’s signal waveforms, it’s usually referred to as power-added efficiency (PAE). When the gain is high enough, the PAE is typically close in value to the amplifier’s efficiency.

To increase efficiency, a Class B PA uses two active devices in what’s often referred to as a “push-pull” configuration. An input signal waveform is power-divided into two signals, with each transistor conducting and amplifying the split half of the input signal wave-

form for one-half the time, or for one-half or 180 deg. of the input waveform cycle. Then the two halves of the amplified signal waveforms are power-combined and reassembled at the output of the PA. The active devices operate with a 180-deg. phase difference so that their outputs can be combined to achieve a maximum total signal level.

Although this amplifier configuration requires more active devices, the devices can be turned off for as much as 50% of the time to approach an efficiency of 78.5% under ideal conditions. However, the high efficiency from the signal processing and device switching results in less linearity than a Class A amplifier.

Class AB amplifiers represent efforts to combine the high linearity of Class A amplifiers with the improved efficiency of Class B PAs. Here, the two active devices are on for more than “just” 50% of the time, creating an overlapping period when both devices are processing an input signal waveform. This produces a longer duration of amplified signal waveform, with the opportunity to achieve smooth transitions between when each active device is driving the input waveform, albeit with some sacrifice in overall gain compared to a Class B PA architecture.

To create greater efficiency, multiple active devices in Class C PAs conduct for less than one-half of the input signal waveform, or less than the 180 deg. of a Class B amplifier configuration, to save power during the process of boosting the input signal waveform.

By operating active devices with conduction angles as low as 80 deg., a Class C amplifier can achieve extremely high efficiency, approaching 90% in some cases. The tradeoff is that turning on and off and switching among multiple active devices results in high levels of distortion and, typically, the need to add resonant circuits to recover amplified circuits. Class C amplifiers are a good fit for applications in which distortion is not critical, such as for powering pulsed radar signal waveforms.



2. Model 3100LA is a robust Class A PA with high linearity from 250 kHz to 150 MHz. (Courtesy of ENI)

Class C amplifier configurations are also used in combination with Class B PAs for a “Doherty” amplifier, which is essentially a Class B amplifier in parallel with a Class C amplifier. The PA operates in Class B most of the time to maintain good linearity. However, during signal peaks, it will draw on the parallel Class C stage to provide higher peak power but with less linearity.

Signals of the two amplifier stages are summed at the output of a Doherty amplifier to achieve high output power with somewhat better efficiency than a standard Class B amplifier. Additional amplifier classes attempt to increase operating efficiency for such applications as battery-powered mobile devices, using switched power supplies and driving signals as pulsed waveforms.

In addition to different amplifier classes for choices of operating behavior, amplifier designers have explored creative circuit techniques to boost efficiency. Solid-state amplifiers tend to operate at high efficiency when its active devices are operating close to compression, and techniques to modulate an amplifier’s load (such as amplitude or phase tuning) have been applied to maintain the devices close to their com-

pression points, although this is more difficult to do over broader bandwidths.

In recent years, envelope tracking is a technique that has been applied to increase amplifier efficiency. The amplifier’s bias energy is dynamically adjusted to maintain the amplifier in its peak operating region, with its active devices as close to compression as possible. Rather than the fixed dc supply to a conventional amplifier, an envelope-tracking PA modulates the power supply to the amplifier with a wide-bandwidth waveform synchronized to the input signal waveform to the PA.

Envelope tracking can be implemented in several ways, by means of detecting and monitoring the characteristics of the input waveform to be amplified. The supply voltage, for example, may be continuously adjusted to track the amplitude of the input waveform. For an amplifier with a high peak-to-average power ratio, envelope tracking may require the use of a power supply with an extremely wide dynamic range to optimize efficiency.

In all classes, impedance matching of an amplifier’s active devices to surrounding input and output circuits and components is critical for optimum

transfer of signal energy to and from an active device and optimum amplifier efficiency. RF/microwave amplifier designers have long relied on the Smith chart for a graphic depiction of a device’s impedance characteristics, and commercial wideband impedance tuners that can adjust impedance to a device while making measurements on a device in an appropriate test fixture with a broadband vector network analyzer (VNA).

Current manufacturers of such devices include Focus Microwaves (www.focus-microwaves.com) and Maury Microwave (www.maurymw.com). Each has extensive lines of fundamental- and harmonic-frequency manual and automatic (controlled with stepper motors) impedance and load-pull tuners. Both companies also offer calibrated impedance tuners for use through millimeter-wave frequencies, to 110 GHz.

NEW FORM OF FEEDBACK

In the future, creative use of energy harvesting will no doubt be applied to increase the efficiency of high-frequency (and even portable audio) amplifiers. Energy harvesting (see “Harvest Energy from RF Sources,” *Microwaves & RF*, January 2019, p. 54) is a way to extract RF power from the environment, such as by receiving and converting transmissions from radio stations. It’s being planned as a major source of power for mobile and portable wireless devices like Internet of Things (IoT) sensors and RFID tags, but it can be designed into the supporting circuitry of RF/microwave PAs to contribute to the overall efficiency.

Because of the heat normally dissipated by an RF PA, alternative energy-harvesting approaches are being developed to boost amplifier efficiency. One of these is the use of a thermoelectric generator to transform the heat generated by an amplifier into electrical energy that can be fed back to the amplifier. In a way, the PAs’ own initial shortcomings in efficiency are actually being used to increase its operating efficiency. **MTW**

From Benchtops to Pockets: The Age of Ever-Shrinking Test Gear

Working with computers and software, USB-powered RF test instruments are bringing measurements with less size and cost than traditional equipment—yet still pack a punch.

Microwave test equipment is gaining in power even as instruments are shrinking in size. Portable spectrum analyzers and oscilloscopes, for example, were once typified by carrying handles and lightweight battery packs; now they include a Universal Serial Bus (USB) for connection to a PC. In combination with available software, modern RF/microwave instruments are making it possible to pack a laboratory worth of measurement capability in a suitcase, and bring high-frequency measurements into the field without losing too much of the power of larger benchtop or rack-mount instruments.

The proliferation of USB RF/microwave test instruments over the last few years has been phenomenal, to the point that almost any measurement function can be contained within a pocket-sized package. Although they still require additional software and computing capability, like a laptop PC, such measuring instruments are every bit equal to the tasks of generating and analyzing signals through the RF and lower-microwave frequency ranges.

However, such equipment still lacks in performance compared to full-sized

rack-mount and benchtop full-sized test instruments at higher microwave and millimeter-wave (mmWave) frequencies—but they are gaining. Although coaxial connectors are available through mmWave frequencies, just interconnections based on waveguide (when required) can be larger than one of today's USB RF/microwave test instruments.

Almost any RF/microwave measurement function is currently available as a USB instrument, perhaps if only with less bandwidth and frequency range than full-sized test instruments. Even a line of USB vector network analyzers (VNAs), such as the TTR500 series from Tektronix (www.tek.com), provide cost-effective, simple-to-perform two-port vector network measurements with a USB connection and control of a laptop computer (*Fig. 1*).



1. Two-port VNAs in the TTR500 series can make S-parameter measurements across a 122-dB dynamic range from 100 kHz to 6 GHz. (Courtesy of Tektronix Inc.)

These pocket-sized instruments can make two-path S-parameter measurements across a 122-dB dynamic range for signals from 100 kHz to 6 GHz. The analyzers are designed to work with the company's VectorVu-PC measurement software and feature an application programming interface (API) for Microsoft Windows operating-system (OS) software.

A company long associated with VNAs, first as Hewlett-Packard Co., then Agilent Technologies, and now as Keysight Technologies (www.keysight.com), has shown it's quite capable at fitting an effective VNA architecture into a USB-powered enclosure. The firm's Streamline Series of P937XA model two-port USB VNAs, although a fraction the size of a benchtop VNA (*Fig. 2*), sacrifice little in measurement capability and accuracy across a total frequency range of 300 kHz to 26.5 GHz.



2. The Streamline Series of USB VNAs covers a total measurement range of 300 kHz to 26.5 GHz. (Courtesy of Keysight Technologies)

A total of six models provide frequency coverage of 300 kHz to 4.5, 6.5, 9.0, 14.0, 20.0, and 26.5 GHz with ± 1 -Hz frequency accuracy. They also achieve dynamic range of better than 114 dB at 9 GHz and better than 110 dB at 20 GHz. These lightweight little VNAs offer fine frequency tuning, with resolution of 1 Hz to 2.5 GHz, 3 Hz to 10 GHz, 6 Hz to 20 GHz, and 12 Hz above 20 GHz. As small as the USB package, the architecture can be expanded to accommodate four-port VNA measurements.

Not to forget one of the “workhorse” instruments at lower frequencies, Keysight also offers its model U2702A 200-MHz USB modular oscilloscope; in appearance, it looks very similar to the USB VNAs. The oscilloscope works with test software running on a PC with the Microsoft Windows 7 or newer OS, using the computer’s display screen to show measured results and the graphical user interface (GUI) for setting up measurements. With 32 Mpoints of memory and a 1-Gsample/s sampling rate, the little USB oscilloscope can hold its own with much larger scopes built for the same test bandwidth.

When it comes to USB and VNAs, few companies can match the choice of instruments offered by Copper Mountain Technologies (www.coppermountaintech.com) and its one-, two-, and four-port USB VNAs for testing through 20 GHz. With instruments for both 75- and 50- Ω measurements, USB VNAs like the 50- Ω model C4420 perform all four S-parameter measurements with measurement speeds as fast as 10 μ s/point and dynamic range as wide as 152 dB. To add to its power, the firm also offers versions of its CobaltFx Frequency Extension System that can bring two- and four-port 9- and 20-GHz USB VNAs much higher in frequency—as high as 110 GHz when needed!

PACKING IT IN

Although many of the latest USB RF/microwave test instruments rely on a USB-connected computer to show

test results, some high-frequency USB instruments truly pack everything into one package, such as the compact handheld spectrum analyzers from B&K Precision Corp. (www.bkprecision.com). The firm’s 2650A series of analyzers cover frequency ranges of 50 kHz to 3.3 GHz or 8.5 GHz, with a tracking generator available for models through 3.3 GHz.

In addition to working with a USB computer, B&K’s spectrum analyzers have a built-in color liquid-crystal-display (LCD) screen with 640- \times -480-pixel resolution and they can operate for as long as 4 h on a battery charge for ease of portable measurements (Fig. 3). They weigh only 4 lbs. (1.8 kg) with the rechargeable lithium-ion battery and deliver measurement capabilities that compare favorably with much larger benchtop spectrum analyzers. Specs include SSB phase noise of -90 dBc at 100 kHz offset from the carrier, displayed average noise level (DANL) of -127 dBm, and fast sweep speeds for performing quick scans for noise and interference.



3. Some USB instruments, such as these handheld spectrum analyzers, can display test results on their own screens in addition to a connected PC. (Courtesy of B&K Precision Corp.)

Among the smallest of USB RF/microwave test instruments, the MA24108A (10 MHz to 8 GHz), MA24118A (10 MHz to 18 GHz), and MA24126A (10 MHz to 26 GHz) true-RMS power sensors from Anritsu Co. (www.anritsu.com) have block diagrams that resemble a measurement bench, with two diode-based signal paths orchestrated by a microcontroller even while they are contained in a housing that fits into a shirt pocket (Fig. 4). These tiny mea-



4. These power sensors are capable of NIST-traceable measurements at frequencies as high as 26 GHz. (Courtesy of Anritsu Co.)

surement tools can be calibrated with traceability to the National Institute of Standards and Technology (NIST). They are complete power measurement systems, with calibration factors and linearity and temperature correction data stored within the sensor.

The two diode detector paths provide measurement options within these test systems, allowing the microcontroller to choose the signal path that maintains the detector diodes within their square-law regions or power level to achieve the highest measurement accuracy. The power sensors can be used with a USB connection to a PC or with selected company handheld power meters. They can make true RMS power measurements for CW, multitone, and digitally modulated signals over a better than 60-dB dynamic range.

Anritsu also offers its ShockLine MS46122B series of USB VNAs with three two-port models covering bandwidths of 1 MHz to 8.0, 20.0, and 43.5 GHz. These compact USB-controlled instruments boast better than 100-dB dynamic ranges and measurement speeds of better than 130 μ s/point, making them well-suited for passive 5G component measurements.

GENERATING SIGNALS

Lest it seem that all USB instruments are for analyzing or measuring RF/microwave signal characteristics, signal generators such as the LSG and LMS series Lab Brick instruments from Vaunix Technology Corp. (www.vaunix.com) provide swept-frequency and CW output signals through 20 GHz with very good spectral purity, including low phase noise. The LSG series of signal

generators are designed for swept-frequency signal generation, while the LMS series instruments provide frequency switching speeds as fast as 100 ms with 100-Hz frequency resolution. They are capable of phase-continuous sweeps and can work with internal or external pulse modulation.

In addition to its compact signal generators, Vaunix has added its LPS line of phase shifters in the same compact housing, with mini-b USB connector and SMA RF connectors (Fig. 5). Mod-



5. Phase shifters such as these operate under USB control at frequencies to 12 GHz. (Courtesy of Vaunix Technology Corp.)

els are available for frequency ranges of 1 to 2 GHz, 2 to 4 GHz, 4 to 8 GHz, and 8 to 12 GHz, each with 1-deg. phase-adjustment resolution and ± 2.5 -deg. phase-adjustment accuracy across a full 360-deg. phase-adjustment range. These phase shifters, which are handy little devices for performing measurements on phased-array antennas and systems as well as phase-sensitive coaxial cables, maintain healthy test-signal power with typical insertion loss of only 5 to 6 dB throughout their frequency ranges.

For those in need of complex modulated test signals, the model VSG-25A from Signal Hound (www.SignalHound.com) truly houses large capabilities in a small package (Fig. 6). This is a 12-b in-phase/quadrature (I/Q) baseband arbitrary waveform generator that can generate analog, digital, and arbitrary output waveforms. It can be clocked from 54 kHz to 180 MHz to produce

an output frequency range of 100 MHz to 2.5 GHz with better than 1-Hz frequency resolution and better than ± 5 ppm/year frequency accuracy.

The VSG-25A boasts a 100-MHz modulation bandwidth and includes the software and API needed to generate any number of advanced modulation formats, such as binary phase-shift keying (BPSK), quadrature phase-shift keying (QPSK), 16-state phase-shift keying, and Gaussian minimum shift keying (GMSK). It can also deliver output sig-



6. This arbitrary waveform generator fits on a "USB stick" but provides complex modulated signals through 2.5 GHz. (Courtesy of Signal Hound)

Test Adapter for 0.5mm Pitch LGA20

High Performance Test System

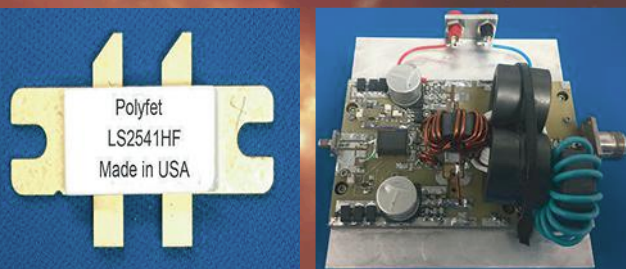
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The USB signal generator is capable of output signal levels from -40 to $+10$ dBm. It features excellent spectrum purity, with SSB phase noise of typically

-88 dBc/Hz offset 1 kHz from a 1-GHz carrier and -132 dBc/Hz offset 1 MHz from the same carrier. It measures just $5.50 \times 2.25 \times 1.0$ in. and weighs a mere 5 oz. The signal generator is designed for use with Microsoft Windows 7.0 or later OS and a USB 2.0 port.

Packing a receiver into the same basic

format, the firm also offers the model USB-SA44B measuring receiver and spectrum analyzer in the same little package. It covers a range of 1 Hz to 4.4 GHz. It's capable of a DANL of -124 dBm/Hz at the lowest frequencies, as good as -158 dBm/Hz at 1 GHz with a built-in preamplifier, and -128 dBm/Hz or better at the highest frequencies with no preamplification. The company's Spike software is compatible with Microsoft Windows 7.0 or higher OS and allows the spectrum analyzer to operate as a real-time spectrum analyzer (RTSA).

For even higher frequencies (through 26.5 GHz), Telemakus LLC (www.telemakus.com) offers a line of frequency-synthesized signal sources in bands such as 700 to 1000 MHz, 1.8 to 2.7 GHz, 9.3 to 10.2 GHz, and 24.0 to 26.5 GHz. The company has extensive lines of RF/microwave instruments with USB ports, including RF/microwave switches through 6 GHz, digital attenuators through 8 GHz, and power sensors covering a frequency range as wide as 50 MHz to 8 GHz. The compact model TED8000-40 power sensor, for example, covers a 40-dB measurement range with 0.5-dB accuracy from 50 MHz to 8 GHz (Fig. 7).



7. One of the earliest suppliers of USB frequency synthesizers is now offering models through 26.5 GHz. (Courtesy of Telemakus LLC)

It should be noted that this is just a sampling of the number of RF/microwave USB test instruments currently on the market—that number continues to climb and with more extending higher in frequency. These handy test tools are a fraction of the size and costs of benchtop measuring instruments, but for those with a PC available, they sacrifice little in performance and accuracy. **ITW**

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Noise Sources in Ultra-Low-Noise Synthesizer Design

This article, the second in a five-part series, focuses in on the synthesizer phase noise sources outside the synthesizer chip, such as noise induced in the voltage-controlled oscillator by power supplies and by the various loop-filter forms.

Phase noise is an interference source and a dynamic range limit in communications systems. The noise can cause interference both “in-channel” for systems with modulation terms close to the carrier, or further from the channel being used in what’s often referred to as adjacent or alternate channel performance.

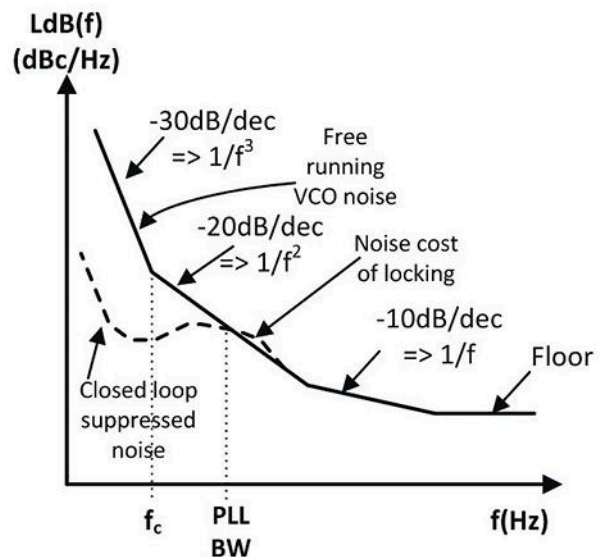
This is the second article in our low-noise synthesizer design series. A moderately longer version will be posted on the *Microwaves & RF* website, and a still more complete version will be posted on the Publications page at www.longwingtech.com. The first article (Ref. 1) covered basic design for functionality and stability. This second article, as well as the upcoming Part 3, will extend the basic methods to specifically cover designing for minimum phase noise. Here, Part 2 focuses on noise sources outside the synthesizer integrated circuit (IC), such as the voltage-controlled oscillator (VCO) and the various loop-filter forms.

The synthesizer IC noise and loop functions for shaping and combining all of the sources will be presented in the next article, revealing how modern synthesizer ICs with on-die VCOs can deliver performance that’s often competitive and sometimes superior to synthesizers with low-noise discrete VCOs. The fourth article in this series will cover parts and CAD tools available to the low-noise synthesizer designer. The fifth and final article will bring this material together in the form of low-noise synthesizer examples.

FREQUENCY-DOMAIN DEFINITION OF PHASE NOISE

We speak of phase noise as the frequency-domain spectral-density noise surrounding the carrier of a frequency source, such as a VCO. It’s described in units of decibels relative to carrier power per Hz, at an offset “f” from the carrier frequency (Fig. 1). Refer to a source such as Ref. 2 for a more detailed definition.

In the shown VCO noise figure, the –30 dB/decade part of the slope below frequency f_c is flicker noise, which is predomi-



1. This is the phase noise of a free-running VCO and a phase-locked VCO. Here, the dB value will be referred to as $L_{dB}(f) = 10\log(L(f))$.

nantly caused by baseband flicker noise in the internal amplifier mixing up around the carrier. The –20 dB/decade slope is a basic indicator of Q in the oscillator loop. The –10 dB/decade part of the slope is typically only seen in very-high-Q oscillators. The floor is generated by the thermal noise raised by the gain and noise figure of the active device.

The phase noise as shown in Figure 1 is single-sided. Consideration of total noise on both sides, the “spectral density of phase fluctuation” needed to convert phase noise to timing jitter, is discussed in the long version.

INDUCED NOISE IN THE VCO

Basic Induced Noise

Noise on the input (steering) voltage of the VCO will induce a sideband-to-carrier spectral component according to:

$$\frac{S}{c} = S_c = \frac{V_n K_{Hz}}{\sqrt{2} f} \quad (1)$$

We shall refer to this important relationship as the “VCO Noise Modulation Function.” This equation is derived by small-signal FM theory. Here, K_{Hz} is the Hz/V steering function of the VCO and V_n is an rms modulating signal. If V_n is an rms spectral noise density, then this sideband-to-carrier becomes a phase noise density and is converted to dBc using $20\log$.

The noise-modulation function may also be used to give a phase-noise term due to noise on the supply through the power supply “frequency pushing” term K_{pHz} . Noise is modulated from this source to phase noise according to:

$$\frac{S}{c} (\text{power supply}) = S_{cp} = \frac{V_{np} K_{pHz}}{\sqrt{2} f} \quad (2)$$

For both input and power-supply noise, a flat noise spectral density will cause phase noise to decline at 20 dB/decade as frequency increases—similar to the most important part of a VCO noise curve. Over this frequency range, a constant (frequency flat) allowed noise density on steering and power nodes to be specified at a level that keeps this noise below the VCO free-running 20-dB/dec noise slope.

LOOP BW AND VCO K_{Hz} EFFECTS ON PHASE NOISE

The existence of the induced noise leads us to beware of noise on the VCO input, and to look for effects caused by such noise as a function of design choices such as loop BW and VCO gain. Well inside the loop bandwidth, such noises are suppressed by phase-locked-loop (PLL) closed-loop action. But at the loop BW, and for as much as a decade past it, we will have such noise sources acting unimpeded in inducing extra VCO noise. We know that the minimum noise we will have driving the VCO input will be given by the thermal noise of the zero resistor R_2 . From the first article, we have this approximation for R_2 :

$$R_2 = \frac{4\pi N \omega_n \zeta}{K_o I_{pd}} = \frac{2N \omega_n \zeta}{K_{Hz} I_{pd}} \cong \frac{N \omega_L}{K_{Hz} I_{pd}} \quad (3)$$

For the resistor thermal noise voltage, we have the standard equation (Ref. 3):

$$V_{nR2} = \sqrt{4kTR_2} \quad (4)$$

In the above, k is Boltzmann’s constant ($1.38E-23$) and T is absolute temperature (290° at room temperature). Putting these two equations together with the induced noise relation (Equation 1), we find the minimum induced phase noise at the loop bandwidth f_L to be:

$$L_{MinInduced}(f_L) = \frac{4\pi kTN}{I_{pd}} \frac{K_{Hz}}{f_L} \quad (5)$$

In the locked loop, the noise at the loop bandwidth is a critical figure of merit. With a low-noise VCO, the induced noise of R_2 is usually an important component of that noise. This induced noise represents a minimum possible noise—even if there were no other PLL noise sources and the VCO were noise-free, this noise would still exist as the cost of locking the VCO.

LEESON’S EQUATION FOR VCO NOISE—AND ITS CONSEQUENCES

The Expanded Leeson Equation

A detailed expression for VCO phase noise is given below, which is an expansion of the famous equation first developed by Leeson (see long form for references) and further expanded upon by numerous authors. This expression is a linear power ratio. Therefore, in converting it to dB, we use $10\log$. We will use the variable “ $L(f)$ ” for linear carrier-to-noise power ratio at offset “ f .” We will use “ $L_{dB}(f)$ ” for the decibel variant.

In this expression, f is offset frequency; f_o is carrier frequency; f_c is the flicker noise corner; k is Boltzmann’s constant; Q is loaded resonator Q ; G is loop gain in compression (the reciprocal of VCO loop loss given by $1 - Q_L/Q_o$); F is noise factor in compression; K_{Hz} is VCO gain in Hz/volt; K_{pHz} is VCO power supply pulling in Hz per volt; V_{n1} is spectral noise density at offset “ f ” on the steering input; V_{n2} is spectral noise density at “ f ” on the power supply; and P_o is the power dissipated within the loop (losses from all sources). More detailed information is provided in the full version at www.longwingtech.com.

$$L(f) \cong \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_o} f_c}{f^3} + \frac{\left(\frac{f_o}{2Q}\right)^2 \frac{GFkT}{2P_o} + \left(\frac{V_{n1}(f)K_{Hz}}{\sqrt{2}}\right)^2 + \left(\frac{V_{n2}(f)K_{pHz}}{\sqrt{2}}\right)^2}{f^2} + \frac{\frac{GFkT}{2P_o} f_c}{f} + \frac{GFkT}{2P_o} \quad (6)$$

Referring VCO Noise to Input

Leeson’s equation and the earlier relationship on induced noise show that VCO noise at any frequency can be referred to the VCO input as a noise voltage that generates that same VCO noise on the output of a noiseless VCO. Given $L(f)$ or $L_{dB}(f)$, we may write for input referred VCO noise V_{nvco} :

$$V_{nvco} = \frac{\sqrt{2} f 10^{\frac{L_{dB}(f)}{20}}}{K_{Hz}} = \frac{\sqrt{2} f \sqrt{L(f)}}{K_{Hz}} \quad (7)$$

Noise on the power supply also generates noise on the VCO output, which will often require ultra-low-noise supplies for the VCO (discussed in Part 4 of the series). This noise may also be referred to the input for modeling purposes according to:

$$V_{npin} = V_{np} \frac{K_{pHz}}{K_{Hz}} \quad (8)$$

In this equation, K_{pHz} is the VCO gain with respect to the power supply input in Hz/V and V_{np} is the spectral voltage noise density of the supply.

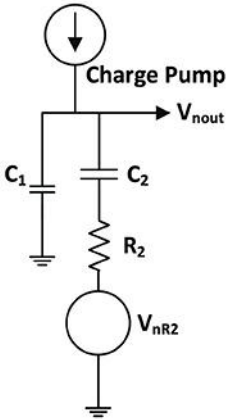
Examination of Leeson's equation shows the noise advantages of higher-frequency VCOs and dividing down in frequency, and of lower K_{Hz} for induced noise. These issues are discussed in more detail in the long version, as is conversion of phase noise to time jitter along with additional noise sources such as resistor excess noise.

FILTER NOISES AND LIMITS

Noise in the loop filter is for the most part suppressed by feedback well inside the loop bandwidth. However, around the loop bandwidth and for up to a decade or so past it, the noise of the filter may dominate the phase noise. As loop bandwidth is directly proportional to R_2 and other resistors in the passive loop filter generally scale with R_2 , the filter noise may set limits on the bandwidth to be used in the PLL. The active loop filter has the advantage that the largest resistor noise will generally be from R_2 , along with the disadvantage of op-amp and reference noises.

Second-Order Passive Filter Noise

The second-order passive filter has the form shown in Fig. 2.



2. Shown is the second-order loop filter with noise.

Analysis of the circuit yields:

$$|V_{noutR2}|^2 = \frac{4kTR_2}{\left(1 + \frac{C_1}{C_2}\right)^2 + (2\pi fR_2C_1)^2} \quad (9)$$

The filter impedance Z_f as seen by the charge pump is:

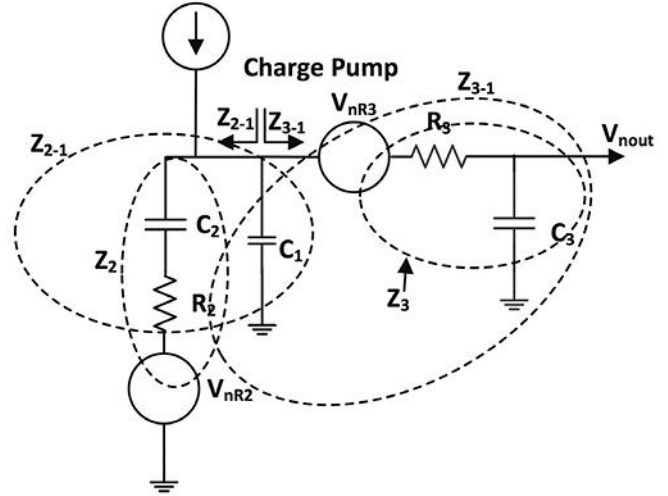
$$Z_f = \frac{sC_2R_2 + 1}{s(sC_1C_2R_2 + C_1 + C_2)} \quad (10)$$

If the noise of the charge pump and dividers is modeled as a noise current I_{pn} , then:

$$|V_{ncp}|^2 = I_{pn}^2 |Z_f|^2 = I_{pn}^2 \frac{\omega^2 C_2^2 R_2^2 + 1}{\omega^4 R_2^2 C_1^2 C_2^2 + \omega^2 (C_1 + C_2)^2} \quad (11)$$

The total filter noise squared is then the sum of these two noises. This form of loop filter represents the lowest possible noise, as it only has R_2 as an internal noise source.

Third-Order Passive Filter Noise



3. Depicted is the third-order passive loop filter with intermediate impedances defined for finding V_{nout} .

Figure 3 shows the third-order passive loop filter. In analyzing for V_{nout} , we define several intermediate impedances. We then apply voltage and current division to the different blocks. Going through this process (see long form for more details), we find the below set of equations:

$$Z_f(s) = \frac{1 + sT_2}{s A_0(1 + sT_1)(1 + sT_3)} = \frac{1 + sC_2R_2}{s(A_2s^2 + A_1s + A_0)} \quad (12)$$

$$T_2 = R_2C_2 \quad (13)$$

$$T_3 = R_3C_3 \quad (14)$$

$$T_{3-1} = \frac{C_1C_3}{C_1 + C_3} R_3 \quad (15)$$

The noise from R_2 at the output is:

$$V_{nout2} = \frac{4kTR_2}{\frac{C_1 + C_3}{C_2} (sT_2 + 1)(sT_{3-1} + 1) + (sT_3 + 1)} \quad (16)$$

The noise from R_3 at the output is:

$$V_{nout3} = \frac{4kTR_3 [C_1(sT_2 + 1) + C_2]}{(sT_3 + 1)[C_1(sT_2 + 1) + C_2] + C_3(sT_2 + 1)} \quad (17)$$

And then finally:

Noise in the loop filter is for the most part suppressed by feedback well inside the loop bandwidth. However, around the loop bandwidth and for up to a decade or so past it, the noise of the filter may dominate the phase noise. As loop bandwidth is directly proportional to R_2 and other resistors in the passive loop filter generally scale with R_2 , the filter noise may set limits on the bandwidth to be used in the PLL. The active loop filter has the advantage that the largest resistor noise will generally be from R_2 , along with the disadvantage of op-amp and reference noises.

$$V_{nout} = \sqrt{V_{nout2}^2 + V_{nout3}^2} \quad (18)$$

Compared to older integer-N designs, both R_2 and thus R_3 are smaller with the lower N value of modern fractional-N synthesizers that have high phase-detector frequencies—and thus have lower noise. Oftentimes, R_3 is in the range of about R_2 to $3R_2$. With the properly designed third-order passive loop filter, we may thus approximate the noise voltage to be about 1.5 to 2 times that of the second-order filter.

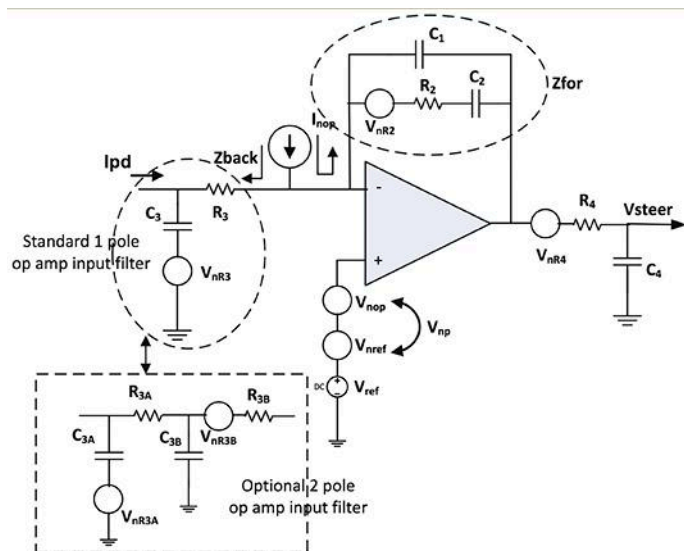
The lower R_2 and R_3 values are factors that contribute to lower total noise. Additional factors are the higher frequency to be divided down to the application frequency and the higher phase-detector frequency and loop bandwidth of the modern sigma-delta PLL (which will be presented in Part 3). For discrete VCOs, lower K_{Hz} allowed by higher voltage is also an essential factor (see long form for analytic details).

Third-Order Buffered Semi-Active Filter

A common active filter strategy is to break the third- or fourth-order passive filter up with an op-amp buffer in the middle that drives the final one or two RC stages, which shall be referred to here as “semi-active.” Since it’s not the most recommended active filter form, the analysis and design of this filter form is deferred to the full version of this article posted on the Longwing website.

Fourth-Order Active Filter Noise

The design methodology for the highly recommended “slow slew mode” fourth-order active filter was given in Part 1 of this series (Fig. 4). This active filter architecture is designed to reduce the bandwidth and slew-rate requirements on the op amp, at which it’s partially successful. The use of the inverting mode with R_2 and C_2 in the feedback path allows this form to provide higher tune voltages with low noise gain. Current flows through R_3 and then through R_2/C_2 to charge up the op-amp output to whatever voltage is needed. The input RC is intended to shield the op amp from the high slew rate and bandwidth of the charge-pump output.



4. The fourth-order active loop filter with option to become fifth-order. The noise sources to be analyzed are shown.

However, it may be advantageous to add an additional input RC stage. As pointed out by Banerjee, experimental evidence (Ref. 4, 5th ed., pp.371-372) indicates that when the op amp in an active loop filter is not fast enough, the $1/f$ noise of the PLL can sometimes increase by several dB. This is presumably due to pulse widening that allows more charge pump $1/f$ noise to go through.

The noise on the steering output of the active filter may be characterized as the sum of the noise powers from the plus input, the minus input, the forward impedance, and in the final RC stage.

The minus input noise is the thermal of R_3 gained up by:

$$V_{nopR3}^2 = 4kTR_3 \left| \frac{Z_{for}}{Z_{back}} \right|^2 \quad (19)$$

We can generate this over frequency using the next several relationships:

A common active filter strategy is to break the third- or fourth-order passive filter up with an op-amp buffer in the middle that drives the final one or two RC stages, which shall be referred to here as “semi-active.” Since it’s not the most recommended active filter form, the analysis and design of this filter form is deferred to the full version of this article posted on the Longwing website.

$$Z_{back} = R_3 + \frac{1}{sC_3R_3} = \frac{sC_3R_3+1}{sC_3} \quad (20)$$

$$Z_{for} = \frac{1+sR_2C_2}{s(C_1+C_2+sR_2C_2C_1)} \quad (21)$$

Next, we consider the gained noise from the plus input of the op amp. This is the gained rms sum of the reference noise and the op amp’s own noise, given by:

$$V_{nopp}^2 = V_{np}^2 \left| 1 + \frac{Z_{for}}{Z_{back}} \right|^2 \quad (22)$$

The below magnitude squared functions are convenient to use:

$$|Z_{back}|^2 = R_3^2 + \frac{1}{\omega^2 C_3^2} = \frac{\omega^2 R_3^2 C_3^2 + 1}{\omega^2 C_3^2} \quad (23)$$

$$|Z_{for}|^2 = \frac{\omega^2 C_2^2 R_2^2 + 1}{\omega^4 R_2^2 C_1^2 C_2^2 + \omega^2 (C_1 + C_2)^2} \quad (24)$$

The noise generated by R_2 is found by taking into account that the minus input of the op amp is a “virtual ground.” Op-amp feedback holds it equal to the plus input. Therefore, noise from R_2 comes straight through to the output except in the case of being filtered within Z_{for} when $C_1 > 0$.

$$|V_{nopR2}|^2 = \frac{4kTR_2}{\left(1 + \frac{C_1}{C_2}\right)^2 + (2\pi fR_2C_1)^2} \quad (25)$$

The noise generated on the op-amp output by the op-amp noise current is again found by noting that the minus input is held equal to the plus input via op-amp feedback. The only way for that to hold is for I_{nop} to flow totally through Z_{for} and not through Z_{back} .

$$|V_{nopInop}|^2 = I_{nop}^2 |Z_{for}|^2 \quad (26)$$

For the sake of convenience, we may count the noise of R_4 as part of the op-amp output. We now have all of the noise terms at the op-amp output.

$$V_{noptot}^2 = V_{nopR3}^2 + V_{nopp}^2 + V_{nopR2}^2 + V_{nopInop}^2 + V_{nR4}^2 \quad (27)$$

This noise needs merely to be passed through a now noiseless R_4/C_4 filter function to provide the noise from the active filter to be presented to the steering input of the VCO.

$$V_{nout}^2 = \frac{V_{noptot}^2}{\omega^2 C_4^2 R_4^2 + 1} \quad (28)$$

With the above, we have all of the major open-loop noises that will be shaped by the loop except for what is sometimes called the “PLL noise.” This is something of a misleading term since it typically means just the noise of the charge pump and dividers in the PLL—not the total PLL noise. It’s not given above in the noise sources review, since it’s normally specified as a closed-loop noise after shaping. It will be covered in Part 3 along with the methods for analyzing how noise is shaped, optimum loop bandwidth, and the synthesizer IC figure of merit for evaluating chip noise. **mw**

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A Brief Tutorial on Microstrip Antennas (Part 4)

Wrapping up this series on microstrip antennas, attention turns to series feeds for microstrip array antennas along with the series/parallel combination technique.

This article picks up where Part 3 left off by diving into the topic of series feeds for microstrip array antennas. The combination of series- and parallel-feed techniques will also be examined.

SERIES FEED FOR MICROSTRIP ARRAY ANTENNAS

In addition to the parallel, or corporate, feed for microstrip antenna arrays, the series feed represents another array implementation method.¹ Figure 1 illustrates the microstrip array series feed with an N -element array, as well as a five-element array featuring the ease with which amplitude taper may be implemented.

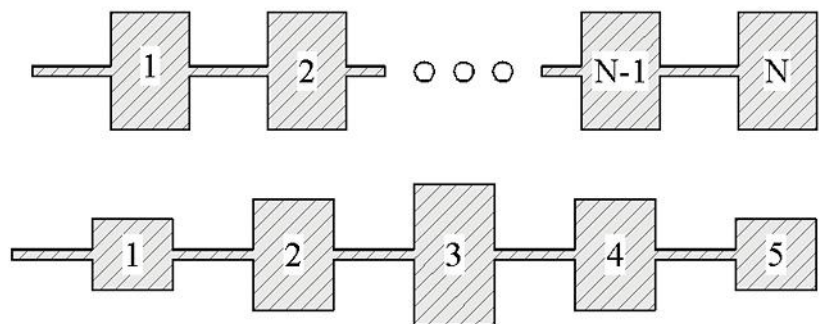
Recall from the introductory material that the width, W , of the conductor is a determining factor with regard to directivity and impedance. It's also instructive to view the equivalent circuit of the series arrangement in combination with admittance elements developed from the transmission line and cavity models (Fig. 2). The equivalent circuit has demonstrated utility in providing reasonable initial values for

the element dimensions and the connecting line impedance.

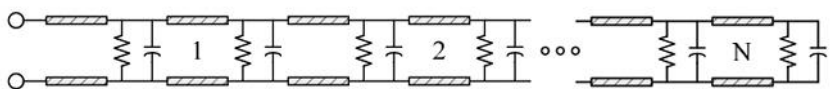
Using the single-element microstrip antenna that was initially investigated and empirical adjustment of element width to produce an amplitude taper, a 1×5 array was constructed and an electromagnetic (EM) analysis executed. The results are graphically illustrated in Table 1.

SERIES/PARALLEL FEED FOR MICROSTRIP ARRAY ANTENNAS

This final example of microstrip antenna arrays will examine the combination of series- and parallel-feed techniques. The series/parallel feed is quite common due to flexibility in the ability to provide amplitude taper and phase progression. The 1×5 series-feed array of the previous section is repeated four



1. Series-feed microstrip arrays include an N -element array, shown on top, while the bottom reveals a five-element array.



2. Depicted here is the equivalent circuit of the series-feed microstrip array.

times to form a 4-x-5 array with amplitude taper in azimuth and no amplitude taper in elevation. The results are summarized in *Table 2*.

As a final example of microstrip antenna-array properties, the previous 4-x-5 array performance is enhanced by amplitude taper in elevation to reduce the elevation beam sidelobes. *Table 3* reveals these results.

Notwithstanding the flexibility and ease of incremental design and analysis, the series/parallel feed of microstrip array antennas is limited, particularly with respect to amplitude taper of the series-feed elements. The limitation in magnitude of the ampli-

tude distribution results directly from the limited sensitivity of the single-element microstrip antenna to variation in conductor width, W . A quantitative evaluation of the sensitivity of microstrip antenna directivity may be attained via numeric evaluation of the single-element directivity equation (Part 2, Equation 7), with W as a variable.

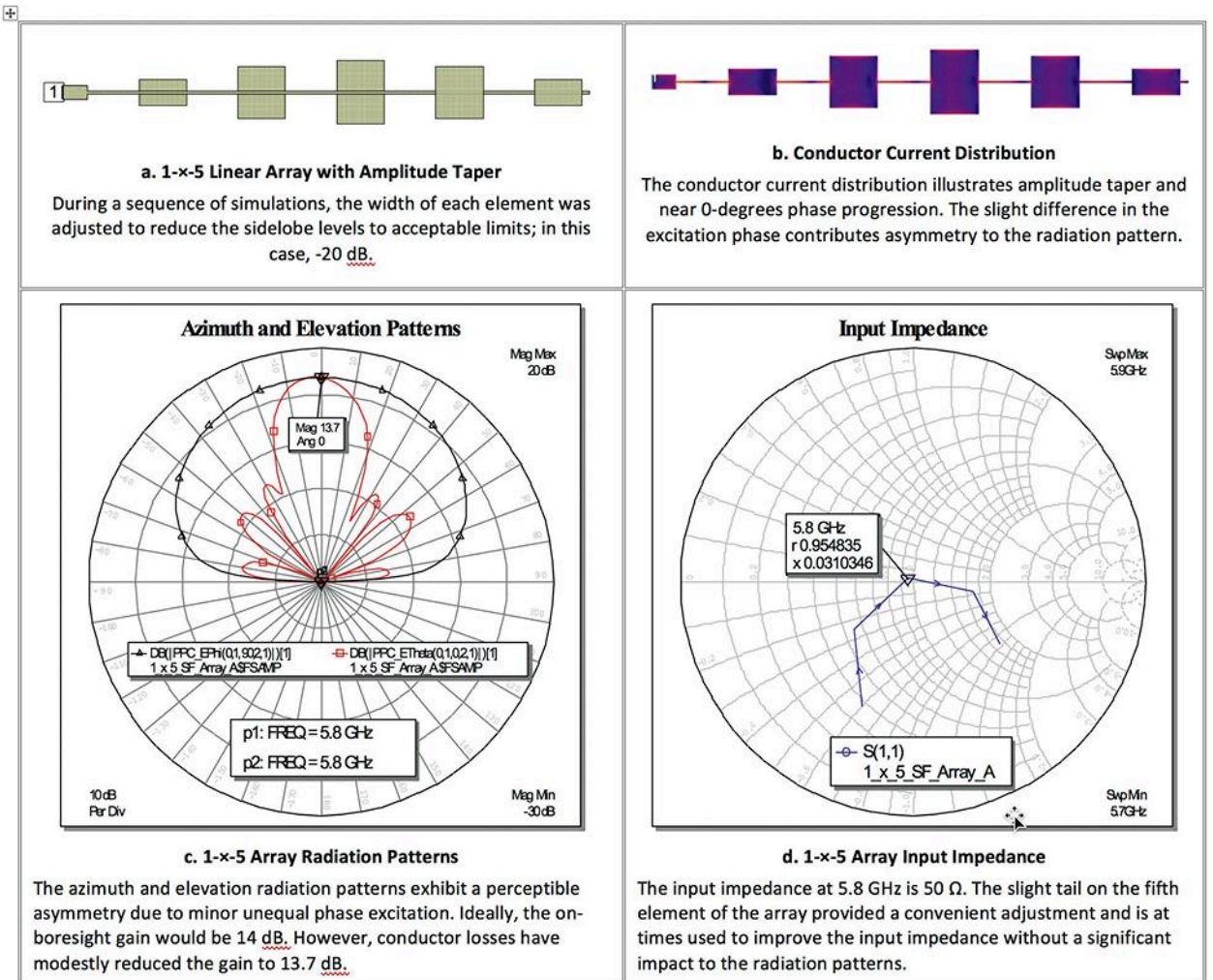
A FINAL NOTE

A judicious approach to the EM simulation of antenna arrays is represented in the incremental analysis structure, i.e., starting with a complete exploration of a single element of the array and

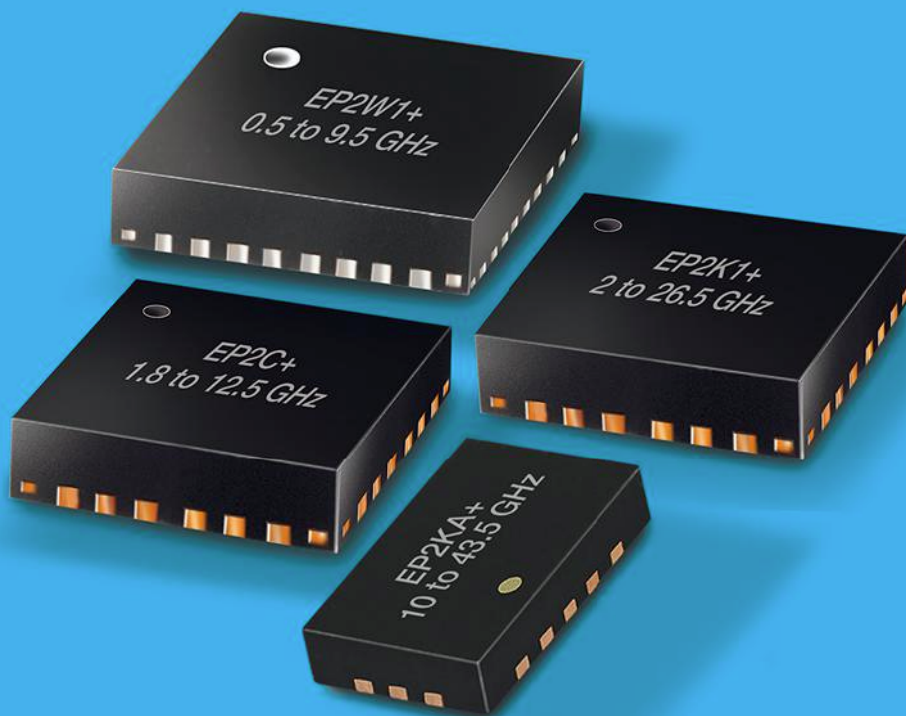
subsequently advancing to additional elements of the rows and columns. The investment of an incremental structure yields benefits in the form of reduced EM analysis time and improved correlation between expected and achievable performance—not to mention reducing the inherent anticipatory stress during simulation execution time.

The discussion related to microstrip antenna feed has been limited to that of the direct feed at the conductor edge, which results in limited operational bandwidth. The operational bandwidth of microstrip antennas can be significantly increased by implementing an aperture coupling below the microstrip

Table 1: 1-x-5 Element Linear Array





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element. The improved performance is accompanied by the added complexity and cost of a dielectric and conductor layer below the radiating elements.

APPENDIX A

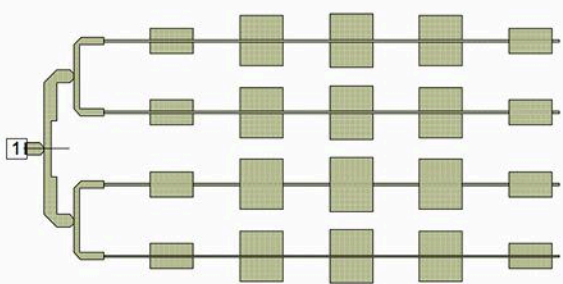
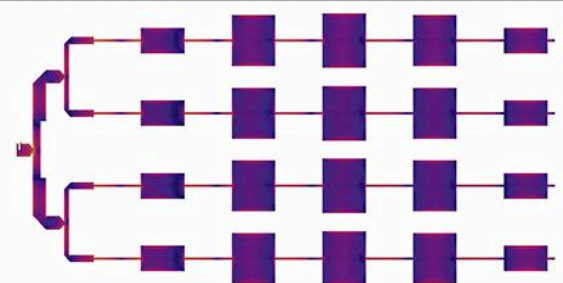
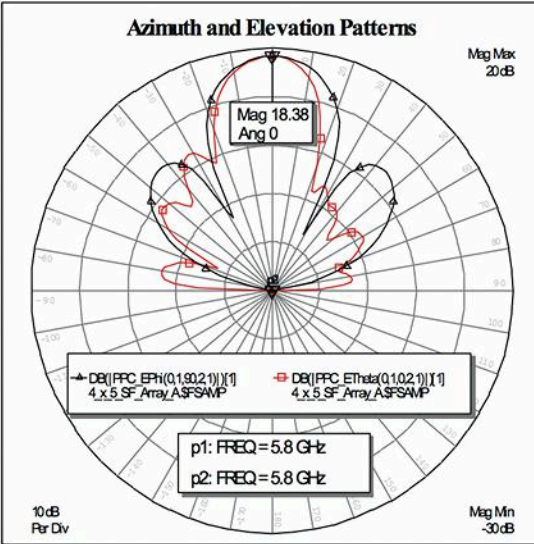
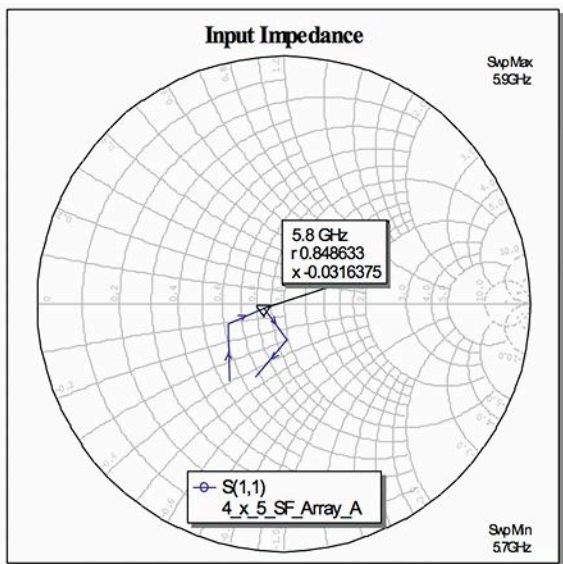
PCAAD 7.0 is a Windows-compatible antenna analysis, modeling, and

design software package. It contains more than 50 routines treating wire antennas, aperture antennas, microstrip antennas, arrays, transmission lines, and waveguides. These routines are integrated into a menu-driven, user-friendly system that facilitates rapid analysis and performance evaluation

of a wide variety of antenna types. PCAAD 7.0 includes a 120-page printed user manual that describes the use of the software, provides examples for each of the routines, and lists technical references.² The PCAAD data output offers an excellent starting point for subsequent EM analysis.

(Continued on page 56)

Table 2: 4-x-5 Element Linear Array with Azimuth Amplitude Taper

 <p>a. 4-x-5 Linear Array with Azimuth Amplitude Taper</p> <p>Each row of the array is fed from the output of an equal amplitude power divider. As a result, each of the 1-x-5 composite arrays has an equal distribution in elevation.</p>	 <p>b. Conductor Current Distribution</p> <p>The conductor current discloses near zero phase excitation. Note the slight advance of the phase excitation at the first element. The non-zero phase excitation contributes to pattern asymmetry.</p>
 <p>c. 4-x-5 Array Radiation Patterns</p> <p>The lower sidelobe levels of the azimuth pattern (red) disclose the amplitude taper. The asymmetry of the azimuth pattern reflects the minor, non-zero phase excitation as evident from the conductor current. The expected gain increase of 6.0 dB over the 1-x-5 array is not realized due to power divider and conductor losses.</p>	 <p>d. 4-x-5 Array Input Impedance</p> <p>The 4-x-5 array input impedance appears well matched; the result of optimization of the 1-x-5 prior to elevation expansion of the array. The bandwidth of the matched impedance may be improved by adjusting the center frequency impedance point to the right in the 1-x-5 array. The input impedance at the band edges is improved with only a slight degradation to the center frequency impedance.</p>

Dealing with Differences in RF Semiconductors

The characteristics of different substrates and device architectures make it possible to reach many speeds and frequencies with modern semiconductor devices and their packages.

Selecting semiconductors for RF/microwave applications involves choosing from among a large array of devices fabricated on different substrates. As the industry hopes to combat the ever-increasing congestion of lower-frequency spectrum with signal bandwidths reaching into the millimeter-wave (mmWave) range, semiconductor materials and devices will be pushed into new regions to achieve more gain and power at higher frequencies.

Bipolar junction transistors (BJTs) fabricated on silicon (Si) substrate wafers—the oldest transistors used in microwave circuits—are still used in both low- and high-power applications. Si bipolar transistors are simple devices that can operate with a single positive voltage supply but provide reasonable gain through RF and lower microwave frequencies.

As with many other high-frequency transistor configurations, BJTs consist of several semiconductor diode junctions, fabricated from layers of p-type and n-type semiconductor materials. The p and the n refer to “positive” and “negative” and denote whether a material has an excess of holes or electrons, respectively. They also indicate how the current will flow in a semiconductor device formed of the materials.



1. This hermetic package holds a high-power, +50-V dc Si bipolar transistor capable of 350 W pulsed output power from 1025 to 1150 MHz for Mode-S aviation radar transmitters. (Courtesy of MACOM)

A BJT has three terminals—the base, collector, and emitter—with the voltage between two of the terminals, such as the base and the emitter, serving to control the flow of current from the other terminal, such as the emitter. The input current to a Si BJT controls the flow of output current. Si BJTs can be fabricated as npn devices, with an n-type semiconductor layer between two p-type layers, or as npn devices, with a p-type semiconductor layer between two high-electron-content n-type layers.

Si has been a long-running starting point for many different types of high-frequency transistors, including the Si metal-oxide semiconductor field-effect transistor (MOSFET) and Si laterally

diffused MOS (LDMOS) transistors. In a Si MOSFET, the three terminals are called the gate, source, and drain. Whereas the gain of a BJT does not fluctuate with bias voltage, the gain of a Si FET can vary with changes in input voltage, which typically results in Si BJTs providing better linearity than Si FETs for a given set of operating conditions.

While major suppliers have supported the different types of FETs based on Si substrates, alternative substrate materials, such as silicon carbide (SiC), are also used to fabricate MOSFET devices with the goal of achieving higher-power-handling capabilities. Cree Inc. and its Wolfspeed (www.wolfspeed.com) power and RF division have developed product lines of high-power, high-voltage MOSFET devices on SiC according to the various benefits of the semiconductor material: high breakdown voltage, higher thermal conductivity than Si, and wider bandgap (for higher voltage and higher power) than Si MOSFETs.

The usable gain of Si-based semiconductors, whether BJTs or FETs, is usually defined by a device’s transition frequency (f_T), the point at which the gain drops to unity. For usable gain in a practical amplifier, the high-frequency limit will be considerably less than f_T , though. Still, f_T is a device performance parameter that can be useful when sorting through different discrete or even IC

While major suppliers have supported the different types of FETs based on Si substrates, alternative substrate materials, such as silicon carbide (SiC), are also used to fabricate MOSFET devices with the goal of achieving higher-power-handling capabilities.

devices when seeking semiconductors for high-frequency amplifiers and other applications.

Si-based transistors with f_T 's of 20 GHz or higher are not unusual, although a circuit with such a device at that frequency will function more as a conductor than an amplifier due to unity gain. The actual upper-frequency limit for a practical power amplifier (PA) or low-noise amplifier (LNA) with a 20-GHz f_T might be more like one-tenth of that frequency, or about 2 GHz where there's still usable gain.

COMPOUND SEMICONDUCTORS

Since the gain of Si BJTs and different types of MOSFETs drops at higher frequencies, over time semiconductor device developers have looked to other substrate materials, notably those with higher electron mobilities to support higher-speed, higher-frequency devices. Compound semiconducting materials having covalent bonds with eight electrons consist of materials with three and five valence electrons. For example, gallium with three valence electrons and arsenic with five valence electrons forms gallium arsenide (GaAs), or gallium and nitrogen (with five valence electrons) forms gallium nitride (GaN).

The high electron mobilities of these semiconductor materials has enabled the fabrication of high-power transistors into the microwave and mmWave frequency ranges. It's also opened the door to small-signal, low-noise transistors well into the mmWave frequency range, to about 150 GHz, for low-noise satellite receivers and other communications radio applications.

GaAs and GaN III-V compound semiconductor materials, as they are

known, are typically combined with other compound materials, such as SiC and aluminum-GaAs (AlGaAs), to improve thermal management of the heat produced by the inefficiencies of different transistor and amplifier architectures (*see p. 34*). Additional semiconductor substrate materials, such as indium phosphide (InP) and silicon germanium (SiGe), have also been used in attempts to fabricate transistors capable of gain at extremely high mmWave frequencies.

Metal-epitaxial-semiconductor field-effect transistors (MESFETs) fabricated on GaAs semiconductor wafers have for decades served both large-signal and small-signal (low-noise) markets in commercial and military applications through microwave frequencies, in both discrete-transistor and monolithic-microwave-integrated-circuit (MMIC) forms. More recently, high-electron-mobility transistors (HEMTs) fabricated on GaN base materials, often with SiC or AlGaAs, have shown some of the capabilities of high-power-density substrate materials like GaN and SiC in the creation of power transistors at microwave frequencies.

SURVEYING EXAMPLES

What kinds of RF/microwave power levels are available from commercial discrete transistors fabricated on the different semiconductor materials and using different device architectures? The simplest answers are that silicon-based devices are capable of very high output power levels but at lower frequencies, while GaAs and GaN transistors may be limited in output power compared to silicon transistors but are usable at much higher frequencies.

Various transistor architectures have evolved over time in attempts to optimize the different semiconductor materials for maximum gain, frequency, and/or output power, such as heterojunction bipolar transistors (HBTs), HEMTs, and LDMOS devices. However, each transistor is different and offers its own set of performance levels to evaluate, with many tradeoffs to consider especially in terms of gain, output power, and frequency.

Silicon bipolar transistors are still used for many RF pulsed and CW applications, largely below 1 GHz, with output-power capabilities depending on frequency and bandwidth. For example, the model MRF10350 Si bipolar transistor from MACOM (www.macom.com) is designed for pulsed PAs, such as in Mode-S aviation radar transmitters from 1025 to 1150 MHz. The silicon-nitride-passivated device, which features a gold-metallized emitter, comes in a hermetic metal flange package (*Fig. 1*) to handle excess heat from high power levels. It's rated for 350 W peak output power when amplifying microsecond-length pulses, and provides at least 8.5-dB gain with 40% efficiency at +50-V dc bias.

At slightly higher frequencies, the model AFV141KH enhancement-mode Si LDMOS transistor from NXP Semiconductors (www.nxp.com) targets pulsed L-band amplification applications from 1200 to 1400 MHz. It runs on a +50-V dc supply and provides as much as 1000 W output power and 16-dB gain with 300- μ s pulses at 12% duty cycle. The LDMOS transistor is supplied in a ceramic flange-mount package.

From the same supplier, but with added integration, the model AFIC31025N is a Si LDMOS device that can be con-

sidered a PA; it consists of several transistor stages with impedance matching to 50 Ω . The output contributions of individual LDMOS devices are combined to achieve higher output power levels within a transistor package.

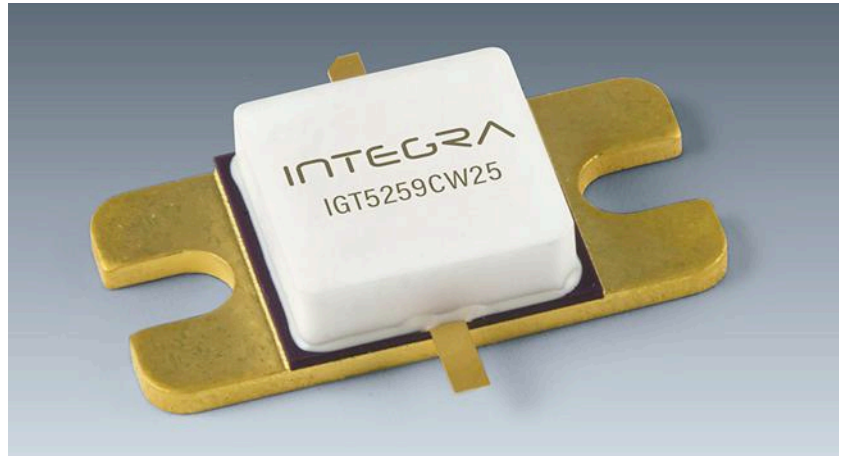
The AFIC31025N operates at S-band from 2.4 to 3.1 GHz and can be used for both CW and pulsed signals. It provides 25 W CW output power from 2.4 to 2.5 GHz with 30-dB power gain. At higher frequencies, it also delivers 25 W output power, from 2.7 to 3.1 GHz, but with 22-dB power gain for 200- μ s pulses at 15% duty cycle. It's designed for maximum operating voltage of +32 V dc and is a good fit for S-band civilian, weather, and maritime radar transmitters. It's supplied in a plastic flange-mount package.

GaAs power transistors are often housed as internally matched devices to optimize output power, such as the model TIM1314-30L from Toshiba Corp. (www.toshiba.com). Supplied in a flange-mount hermetic package, it supplies +45 dBm (32 W) output power at 1-dB compression from 13.75 to 14.50 with 5-dB gain. Designed for +10-V dc operation, it maintains gain flatness of ± 0.8 dB or better across its bandwidth, with PAE of typically 22%.

Of course, GaAs transistors may more commonly be found in LNAs, such as the model MGF4964BL from Mitsubishi Electric Corp. (www.mitsubishielectric.com), which is a GaAs HEMT that's usable to about 25 GHz. It's housed in a plastic Micro-X package since it offers negligible output power. Where it excels is at the receive side of systems, with a typical noise figure of a mere 0.65 dB at 20 GHz, and associated gain of 13.5 dB at 20 GHz.

GOING WITH GaN

Integra Technologies (www.IntegraTech.com), which offers an extensive line of Si LDMOS discrete and integrated devices, has developed packaged transistors based on GaN-on-SiC substrates for higher-frequency operation. One example is the IGT5259CW25 (Fig. 2), which delivers



2. Housed in this package is a GaN-on-SiC discrete +36-V dc transistor capable of 25 W CW output power from 5.2 to 5.9 GHz with 12-dB power gain. (Courtesy of Integra Technologies)

25 W CW output power from 5.2 to 5.9 GHz with 12-dB power gain. It provides 48% typical efficiency when operating from a +36-V dc supply and within-package matching to 50 Ω . It can also be used in pulsed applications and provides 50 W output power and 14-dB gain when handling 1-ms pulses at 15% duty cycle and 80 W output power and 13-dB gain with 300- μ s pulses at 10% duty cycle.

The company also demonstrates what GaN-on-SiC transistors can do at higher frequencies with its model IGT1112M90, which is rated for 90 W peak output power from 11 to 12 GHz. It achieves somewhat lower efficiency at these higher frequencies, at typically 37%, but still provides 9-dB power gain for 150- μ s pulses at 10% duty cycle.

Curiously, Integra offers both Si LDMOS and GaN on SiC packaged transistors for the same frequencies and operating conditions (same applications), allowing customers to specify their technology of choice between two very similar transistor devices. As Chris DeMartino explained in last month's editorial (*Microwaves & RF, January 2019, p. 13*), GaN has benefits at higher frequencies, but when Si, GaN, and even GaAs devices are compared under similar conditions and device architectures, there's often very little separating the semiconductor materials.

Both the Si LDMOS model ILT2731M and the GaN/SiC IGT2731M130 from Integra are designed for pulsed use from 2.7 to 3.1 GHz. When characterized with 300- μ s pulses at 10% duty cycle across that 400-MHz bandwidth, each device delivers 130 W peak output power, although with differences in gain and efficiency. The Si LDMOS device provides 12-dB gain and 43% PAE when operating from a 32-V dc supply, while the GaN/SiC device delivers 15-dB gain with 50% from a higher-voltage +50-V dc supply. If anything, for two devices optimized for the same 2.7-to-3.1-GHz range, the comparison shows the higher-energy, higher-frequency potential of GaN semiconductor materials.

For those interested in the latest developments in wide-bandgap semiconductor technology, the Power Sources Manufacturers Association (PSMA) Semiconductor Committee is sponsoring three industry sessions at APEC 2019 (March 19-21, 2019, Anaheim Convention Center). The sessions explore the rapid emergence of wide-bandgap semiconductors as a significant power-conversion technology. The sessions cover switching and high-power generation for wide-bandgap devices, including GaN and SiC power semiconductors. 

Waveguide Filters Sort Millimeter-Wave Signals

These rugged rectangular waveguide filters provide low-loss passbands from 27 to 86 GHz for a growing number of applications at mmWave frequencies.

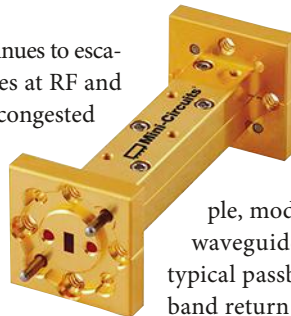
Demand for higher frequencies continues to escalate as relatively lower frequencies at RF and microwave bands become more congested with countless personal communications applications. Responding to that demand, even long-time suppliers of RF/microwave components, such as Mini-Circuits, are reaching higher in frequency, teaming with outstanding engineering partners such as Virginia Diodes (www.vadiodes.com) on a line of waveguide bandpass filters (BPFs) with sharp cutoff responses for passbands from 27 to 86 GHz.

These are almost “textbook” BPFs, with high stopband rejection, low passband loss, and abrupt transitions from passbands to stopbands. Millimeter-wave (mmWave) frequencies are moving quickly from the laboratory to the production line for such applications as short-range, high-data-rate communications links, 5G cellular communications, and radar systems in automotive safety systems. In turn, these filters provide practical solutions for sorting and separating those mmWave signals without penalties in amplitude.

Virginia Diodes (Charlottesville, Va.) brings expertise in the design and development of mmWave- and terahertz-frequency devices, components, and systems, including mixers, detectors, and frequency multipliers for systems and test equipment. The company began with strong interests in the use of higher-frequency electronics for astronomy. In recent years, however, the growing use of wireless applications has pushed the application of electromagnetic (EM) energy onward through the THz range. And, now, teaming with Mini-Circuits has resulted in a rugged, practical line of waveguide BPFs that are well-suited for test, research, and communications systems use.

The WVBP Series of rectangular waveguide BPFs (see figure) are precision-machined components built to handle the demands of attach/detach test and communications-systems applications while contributing minimal distortion. The devices feature sharply defined passbands (see table) with low passband loss through 86 GHz.

The 50- Ω , RoHS-compliant waveguide filters achieve rapid transitions from rejection bands to passbands, with impressive loss behavior throughout the series of filters. For exam-



This precision machined and plated rectangular waveguide filter is an example of the WVBP Series of mmWave bandpass filters for passbands from 27 to 86 GHz.

ple, model WVBP-283-WR28+ is the lowest-frequency waveguide BPF, with a passband of 27.5 to 28.35 GHz, typical passband insertion loss of 0.5 dB, and typical passband return loss of 18 dB. It blocks unwanted out-of-band signals by means of typical lower stopband rejection of 65 dB at 22 GHz and 30 dB at the 27-GHz point, just below the passband. Just above the passband, the upper stopband rejection rises very quickly, typically 39 dB at 28.85 GHz, and still 31 dB at the upper stopband measuring point of 38 GHz.

The highest-frequency filter, model WVBP-833-WR-12+, has a passband of 81 to 86 GHz. Typical passband insertion loss is 0.5 dB while typical passband return loss is 26 dB. Typical lower stopband rejection is 90 dB at 60 GHz and 38 dB at 70 GHz, while typical upper stopband rejection is 26 dB at 88 GHz and 49 dB at 90 GHz. In between, several filters are available for different passbands, such as the model WVBP-383-WR28+ with a passband of 37 to 40 GHz, the model WVBP-673-WR12+ with passband of 64 to 71 GHz, and the model WVBP-783-WR12+ with passband of 76 to 81 GHz.

All of the filters share the characteristics of sharp transitions from passband to stopbands, low passband insertion loss (typically 0.5 dB and no higher than about 1.0 dB even for the highest-frequency models), and low passband return loss (typically 26 dB even for the highest-frequency models).

If anything, Mini-Circuits and Virginia Diodes joining forces creates a path toward bringing mmWave filtering “to the masses,” whether for installation in systems or use in test setups. The move upward in frequency is all but inevitable, given the growing consumption of available frequency bands, and these filters provide the performance at mmWave frequencies that Mini-Circuits’ customers have come to expect for 50 years at lower frequencies. **mmw**

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Switch Drivers Help Accelerate Transitions

These simple-to-apply, efficient high-speed switch drivers are packaged control units for a line of integrated PIN diode RF/microwave switch devices.

Switch drivers are often overlooked among the circuitry in high-speed, high-frequency circuit boards. However, they are essential components for controlling the operation of semiconductor devices, such as PIN diodes. In terms of speed, repeatability, and reliability, RF/microwave signal switching depends on durable switch drivers such as the models MADR-011020 and MADR-011022 from MACOM Technology Solutions Inc. (www.macom.com).

Optimized for use with the company's AlGaAs and HMIC PIN diode switches, these negative-voltage drivers enable extremely fast switching speeds but with very simple component layouts for low-cost switching solutions in both commercial and military applications. The two driver models support medium- and low-power switching circuits with almost negligible propagation delays and minimal quiescent current.

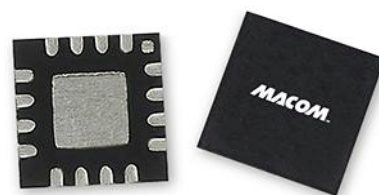
Each switch driver model is supplied in a 4 × 4-mm, 16-contact, power quad flat no-lead (PQFN) package (see figure) to save space in a circuit with a single-pole, double-throw (SPDT) switch. Model MADR-011020 is designed for medium-power applications, providing back-bias voltage selection from -20 to -50 V dc. Also, as much as 50 mA of sinking and sourcing bias current is available for SPDT PIN diode switches or integrated-circuit (IC) PIN diode switches fabricated with the firm's het-

erolithic-microwave-integrated-circuit (HMIC) process.

The switching speed of the MADR-011020 driver and its associated switch (propagation delays) is less than 60 ns when driving a 10-pF capacitive load. The switching speed is considered as the "on" time from 50% of the control signal to 90% of the control voltage, or the "off" time from 50% of the control signal to 10% of the control voltage.


The model MADR-011022 switch driver provides back voltages from -10 to -25 V dc with as much as 25 mA sinking current and 20 mA sourcing current for lower-power SPDT AlGaAs PIN diode and HMIC switches. Both switch drivers have built-in power sequencers to eliminate the need for external power sequencers (and simpler circuit layouts). The internal power sequencers can be operated with standard transistor-transistor-logic (TTL) programmable control. The switching speed of the MADR-011022 switch driver and its associated PIN diode switch is less than 80 ns from an "on" or "off" control signal to 90% or 10%, respectively, of the control voltage.

Single switch drivers are designed for use with the firm's line of HMIC SPDT PIN diode switches, with complementary output ports that provide as much as 25 mA sinking current and 20 mA sourcing bias current to the switches. For added flexibility, the drivers have an extra control pin so that two drivers can work together in parallel to oper-



A pair of negative-voltage switch drivers provide fast switching speeds for a line of SPDT AlGaAs HMIC PIN diode switches.

ate higher-order switch configurations, such as single-pole, three-throw (SP3T) and single-pole, four-throw (SP4T) switches. Compatible AlGaAs HMIC PIN diode switches are available for frequencies through 26 GHz.

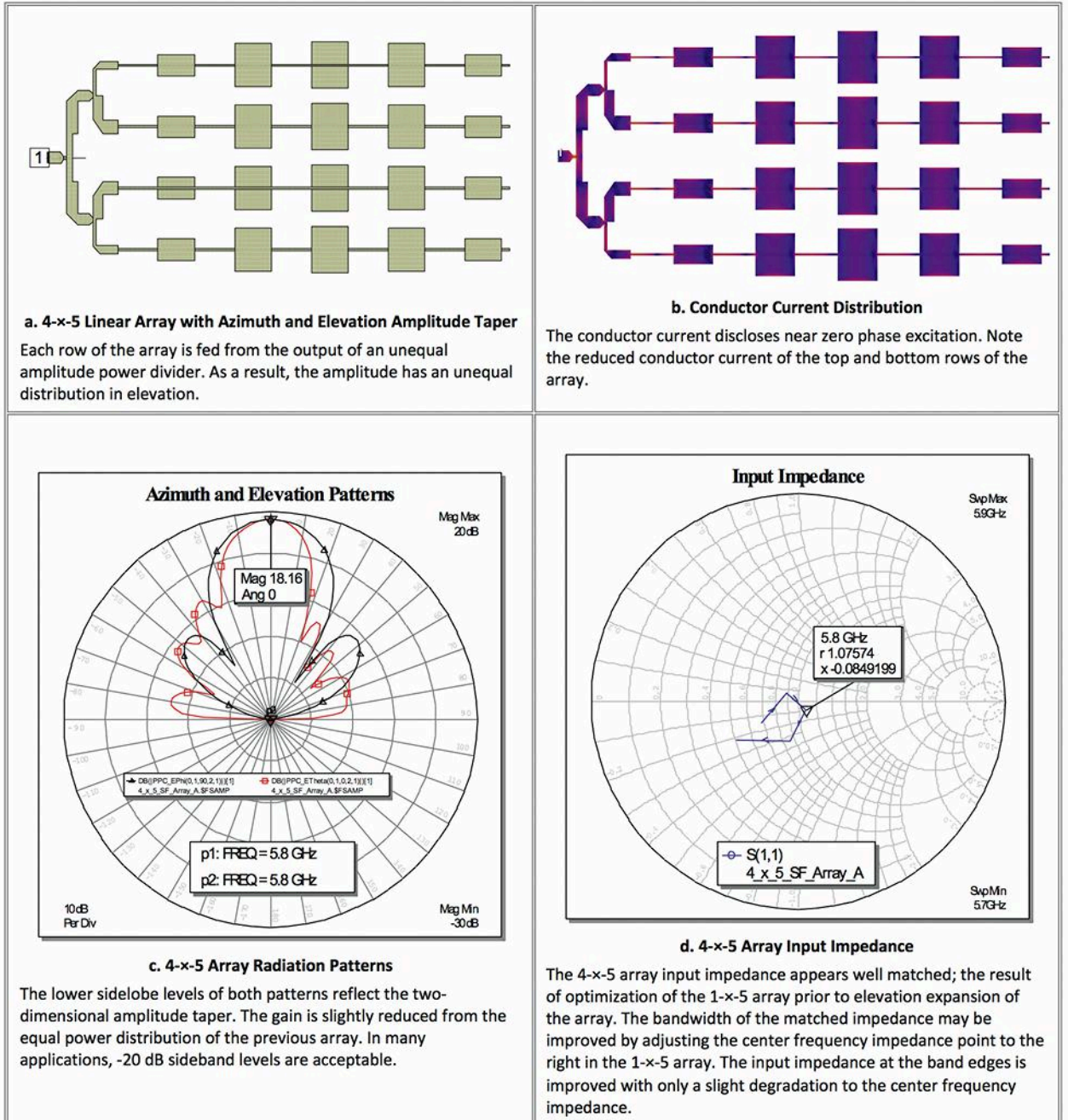
In companion with the firm's line of AlGaAs HMIC PIN diode switches, these packaged driver devices are very energy-efficient for use with many different power supplies. The enable pins on each switch driver can be employed to realize a simple, "all-off" switching state with associated switches. The switch drivers contribute very little energy waste in 50-Ω circuits, with less than 1 mA quiescent current under typical operating conditions. The lead-free, RoHS-compliant switch drivers are designed for operating temperatures from -40 to +85°C and are suitable for commercial and military applications. 

MACOM TECHNOLOGY SOLUTIONS INC., 100 Chelmsford St., Lowell, MA 01851; (800) 366-2266, (978) 656-2500, FAX: (978) 656-2804, www.macom.com

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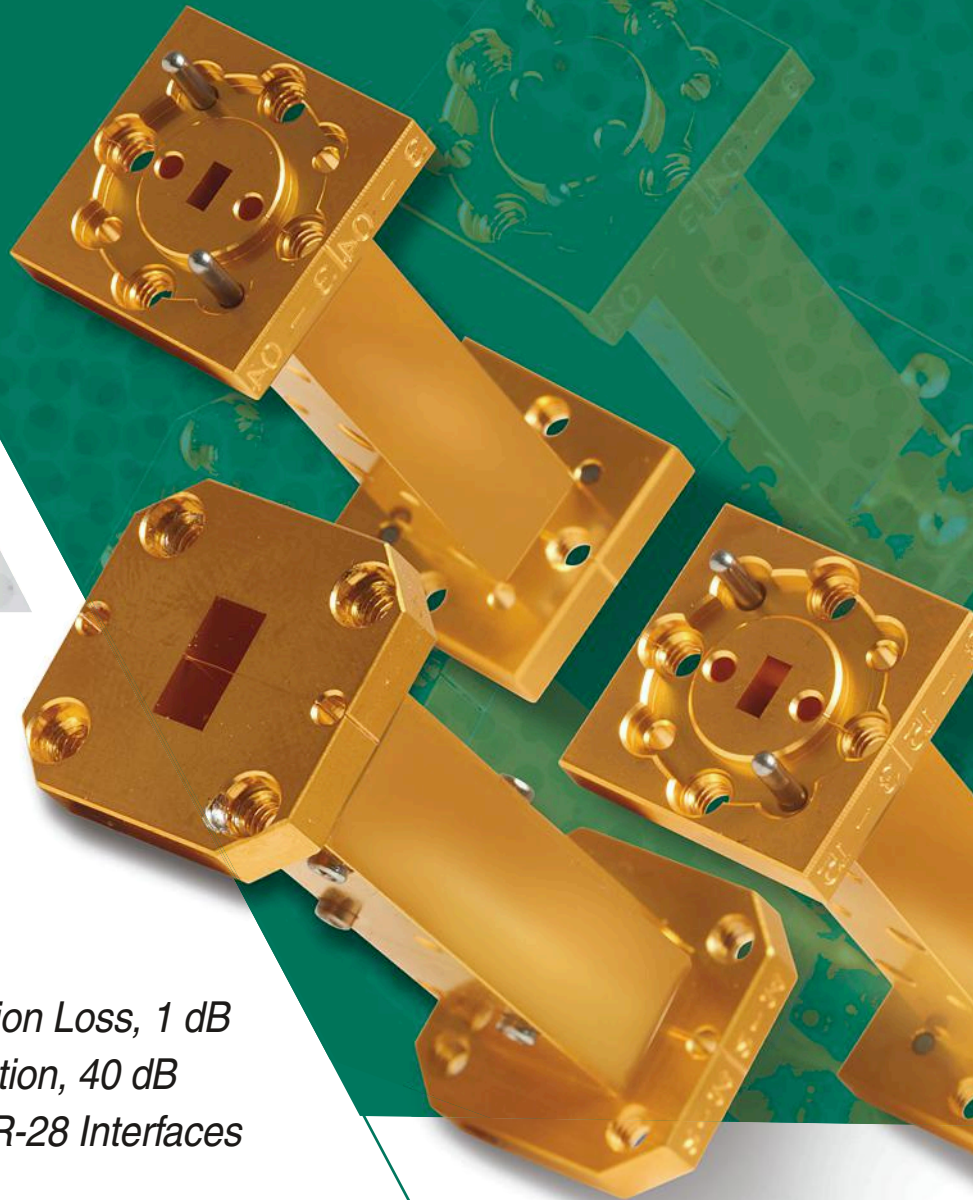
A judicious approach to the EM simulation of antenna arrays is represented in the incremental analysis structure, i.e., starting with a complete exploration of a single element of the array and subsequently advancing to additional elements of the rows and columns.

Table 3: 4-x-5 Element Linear Array with Azimuth and Elevation Amplitude Taper



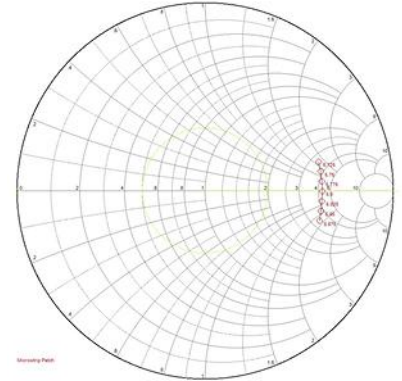
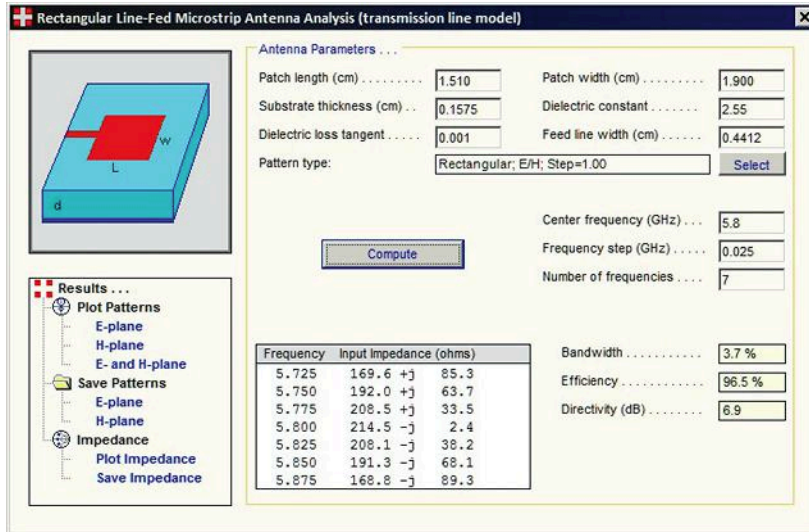
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3. The portion on the left shows rectangular microstrip antenna data entry and calculation, while the resonant impedance of 215 Ω at 5.8 GHz is noted on the portion on the right.

Figure 3 gives details of the rectangular microstrip antenna using a transmission-line feed. Note that the input impedance calculation is 215 Ω versus the calculation of 228 Ω based on the previous equation from Part 1. [11]

REFERENCES

1. The series-fed array is also referred to as a traveling-wave antenna.
2. Additional information is available at the Antenna Design Associate website: <http://antennadesignassociates.com/pcaad7.htm>.

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PTC Mathcad is an engineering math software program that enables computation and analysis using simplified data and formula entry. Additional information may be accessed at <https://www.ptc.com/en/products/mathcad>.

APPENDIX B

1. calculate the line width: (Balanis and Bancroft) $W_{mm} := \frac{c}{2 \cdot f_0} \cdot \sqrt{\frac{2}{\epsilon_r - 1}} = 19.412 \text{ mm}$ - optimized: 19.05 mm

2. calculate the effective dielectric constant: $\epsilon_e := \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \cdot \frac{1}{\sqrt{1 + 12 \cdot \frac{h}{W}}} = 2.327$

3. calculate the length extension: $\Delta L := 0.412 \cdot \frac{(\epsilon_e + 0.3) \cdot \left(\frac{W}{h} + 0.264\right)}{(\epsilon_e - 0.258) \cdot \left(\frac{W}{h} + 0.80\right)} \cdot h = 0.79 \text{ mm}$

4. calculate the length: $L_{mm} := \frac{c}{2 \cdot f_0 \cdot \sqrt{\epsilon_e}} - 2 \cdot \Delta L = 15.375 \text{ mm}$ - optimized: 15.621 mm

5a. calculate the radiation conductance of single slot: (Balanis) $G_{I1} := \frac{I_1}{120 \cdot \pi^2} = 1.431 \times 10^{-3}$

5b. calculate the mutual conductance of the radiating slots: $G_{I2} := \frac{1}{120 \cdot \pi^2} \cdot \int_0^\pi \left(\frac{\sin\left(\frac{k_0 \cdot W}{2} \cdot \cos(\theta)\right)}{\cos(\theta)} \right)^2 \cdot j0(k_0 \cdot L \cdot \sin(\theta)) \cdot \sin(\theta)^3 \cdot d\theta = 5.851 \times 10^{-4}$

5c. calculate the resonant input resistance: $R_{in} := \frac{1}{2(G_{I1} + G_{I2})} = 248.028 \cdot \Omega$ - note + sign for TM₁₀ mode

6. calculate the qtr-wave transformer impedance: $Z_{qT} := \sqrt{50 \cdot R_{in}} = 111.4 \cdot \Omega$ - optimized: 110 Ω

9. calculate the qtr-wave transformer length: $\theta_1 := \frac{\lambda_0}{4 \cdot \sqrt{\epsilon_e}} = 8.477 \text{ mm}$ - optimized: 6.73 mm

10. calculate the directivity: - the directivity of a single slot: $L_E := L + 2 \cdot \Delta L = 17.0 \text{ mm}$

$D_1 := \frac{4 \cdot W^2 \cdot \pi^2}{I_1 \cdot \lambda_0^2} = 3.28$

$J_2 := \int_0^\pi \int_0^\pi \left(\frac{\sin\left(\frac{k_0 \cdot W}{2} \cdot \cos(\theta)\right)}{\cos(\theta)} \right)^2 \cdot \sin(\theta)^3 \cdot \left(\cos\left(\frac{k_0 \cdot L_E}{2} \cdot \sin(\theta) \cdot \sin(\phi)\right) \right)^2 \cdot d\theta \cdot d\phi = 3.488$

- the directivity of a two-slot array: $D_2 := \left(\frac{2\pi W}{\lambda_0} \right)^2 \cdot \frac{\pi}{I_2} = 5.008$ $D_{2,dB} := 10 \cdot \log(D_2) = 7.0 \text{ dB}$

Pushing Process Equipment Forward



In this Q&A, Dr. Ajit Paranjpe, chief technology officer at Veeco Instruments, discusses topics ranging from gallium-nitride technology to advanced packaging.

Can you tell us a little about Veeco?

Veeco designs and manufactures materials engineering and thin-film process equipment for high-tech electronic-device production and development worldwide. Since our IPO in 1994, we have delivered innovative metal-organic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), atomic layer deposition (ALD), advanced packaging lithography, laser annealing, 3D inspection, ion beam, solvent etch/clean, and related technologies to our valued customers.

What markets are being enabled by the company?

Veeco's innovations are used in the development of advanced compound semiconductor products for solid-state lighting/displays (e.g., micro LED) as well as power/RF (e.g., HEMTs for 5G); photonics for 3D sensing (e.g., VCSEL, LiDAR, and augmented reality) and data communications (e.g., Big Data and autonomous vehicles); and advanced semiconductor devices for logic and memory applications (e.g., AI and IoT).

Can you explain what Veeco is doing in terms of GaN-on-Si development?

Recent industry efforts to effectively grow gallium-nitride (GaN) layers on silicon substrates (GaN-on-Si) are finally paying off. However, there are some gaps to be aware of, including the cost of epitaxy and downstream device processing and packaging. Other issues include charge trapping and current collapse, which are being actively resolved to meet reliability targets.

To make significant inroads into GaN Power and RF applications, next-generation production systems using Si substrates need to be adaptable to a wider process window and offer the highest throughput combined with the lowest cost of ownership. These known gaps imply stringent requirements on epi quality.

Veeco is at the forefront of GaN-on-Si development in collaboration with leading device companies and research institutes. First, the epitaxy layers, which often include superlattices, must be deposited with excellent thickness and composition uniformity across the wafer. Customers also demand accurate dopant control with sharp interfaces to optimize the device

properties. There can be zero memory defects to effectively incorporate dopants such as Mg and Fe in specific layers.

Veeco is helping customers solve tough challenges of transistor performance, RF loss, harmonic distortion, and device reliability by leveraging its single-wafer TurboDisc technology that provides industry-leading dopant control and compositional uniformity while reducing the epitaxial growth cost-per-wafer. This is achieved by leveraging the Propel MOCVD system's superior film-deposition control for high-quality buffer growth and its capability to incorporate such dopants.

What do you think the future holds for GaN technology?

GaN's advantages enable high-current density and fast switching with low on-resistance, enabling smaller footprint devices with high temperature operation and the lowest conduction and switching loss. As mentioned earlier, while this brings significant opportunities and advantages to compound semiconductor manufacturers, the form factor and power gains come with associated challenges.

GaN industry forecasts have been pushed out over the last few years because of integration and reliability issues. Traditional players continue to hedge their bets by investing in silicon carbide (SiC). But incumbents, as well as innovative market entrants, are increasingly investing in GaN. The need for high efficiency, high frequency, and small form factors bode extremely well for GaN moving forward.

According to Yole, in the power IC segment, the market is expected to grow at 82% CAGR, from \$18 million in 2017 to \$445 million in 2022. While most devices are still concentrated in the low-voltage category (≤ 200 V), many customers have qualified mid-voltage (600/650/700 V) devices for power supplies in data centers and EV/HEV converter applications.

In RF, the ambitious scope of 5G promises to transform cellular communications, creating new opportunities for

wireless carriers and service providers. Such a high-speed network is currently being planned with a vision of >10 -Gb/s transmission speeds for mobile broadband (phones/tablets/laptops) and ultra-fast, low-latency performance for IoT applications (V2X communications).

GaN is slowly replacing silicon in specific wireless applications (e.g., RF power amplifier front ends of 4G/LTE base stations), and next-generation 5G deployment will involve additional use of GaN technology. Before 5G, there was increased use of GaN-on-SiC in the macro cell. 5G will bring in GaN-on-Si to rival GaN-on-SiC designs with inroads into the small-cell space (micro and metro cells) before potentially overlapping into femtocell/home routers and handsets.

Tell us about the company's advanced packaging technology.

Veeco's advanced packaging portfo-

lio includes the flagship AP300 lithography stepper built on the company's customizable Unity Platform, delivering superior overlay, resolution, and sidewall profile performance and ability to process bowed/warped wafers. This combination enables highly automated, cost-effective manufacturing valued by foundries and outsourced assembly and test (OSAT) providers in advanced logic/memory packaging applications such as fan-in wafer-level packaging (FIWLP), fan-out WLP (FOWLP), through-silicon via, silicon interposer, and copper (Cu) pillar bumping.

In terms of AP outlook, 5G implementation is expected to begin driving production ramps in the Q3 2019 timeframe. Server/cloud industry Big Data, AI, and edge-computing demands will require more processing power and higher bandwidth memory, driving demand for silicon interposer and fanout on substrate solutions. **tmw**



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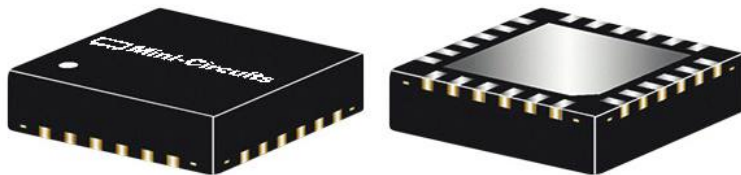
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New Products

Broadband 10-dB Coupler Connects 6 to 18 GHz

THE EDC10-183+ FROM Mini-Circuits is a miniature directional coupler with frequency range of 6 to 18 GHz. It maintains 10-dB coupling with typical coupling flatness of ± 0.7 dB across the frequency range, with directivity of typically 16 dB from 6 to 10 GHz and 18 dB from 16 to 18 GHz. The GaAs-based, 50- Ω coupler cuts mainline insertion loss to typically only 1.0 dB from 6 to 10 GHz, 1.3 dB from 10 to 14 GHz, 1.4 dB from 14 to 16 GHz, and 1.5 dB from 16 to 18 GHz. It features excellent return loss at all three ports, 22 dB or better from 6 to 10 GHz. The RoHS-compliant directional coupler provides a quadrature phase shift between through and coupled signal paths. It's housed in a 24-lead, 4- x 4-mm surface-mount package and designed for operating temperatures from -40 to $+85^\circ\text{C}$.

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MINI-CIRCUITS MODEL ZCDC10-K0644+ is a dc-pass 10-dB directional coupler with coupling flatness of typically ± 0.4 dB across a wide frequency range of 6 to 40 GHz. Suitable for test-and-measurement and power-monitoring applications, the RoHS-compliant, 50- Ω coupler handles input power levels to 17 W with low mainline insertion loss of typically 0.8 dB from 6 to 18 GHz and 1.2 dB or less from 18 to 40 GHz. The directivity is typically 26 dB from 6 to 18 GHz and typically better than 20 dB from 18 to 40 GHz. Input and output port return losses are typically 29 dB from 6 to 18 GHz and typically 24 dB or better from 18 to 40 GHz,

while coupled-port return loss is typically 26 dB from 6 to 18 GHz and 21 dB or better from 18 to 40 GHz. The coupler is 1.25 x 0.63 x 0.50 in. (31.75 x 16.0 x 12.7 mm) without measuring the connectors and can be supplied with female SMA or female 2.92-mm coaxial connectors. It's designed for operating temperatures from -55 to $+100^\circ\text{C}$ and can pass as much as 0.6 A current from input to output.

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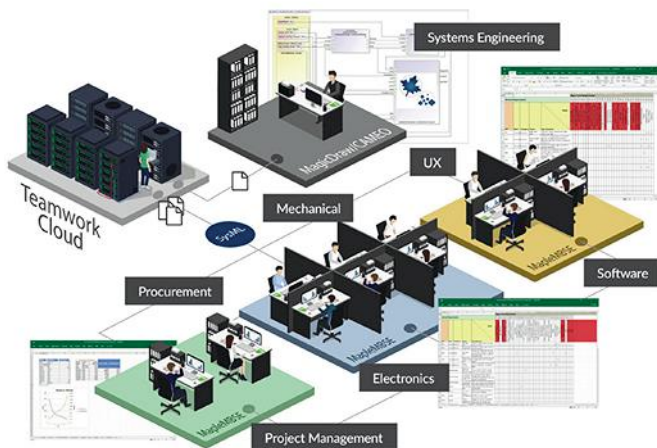
output ports. The amplifier measures 19 x 12.25 x 24 in. and weighs 90 lbs.

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and improve the design. By connecting MapleMBSE to Teamwork Cloud, a model-management system, it's possible to access models created in several different tools, including MagicDraw, and Cameo Systems Modeler. MapleMBSE can also be integrated directly with other SysML-based tools, such as IBM Rational Rhapsody. The new software is one of many Maplesoft products and services used in machine design, robotics, aerospace, automotive, industrial automation, and many other fields.

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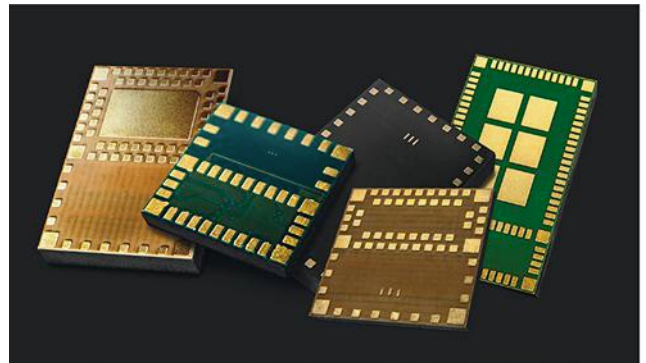
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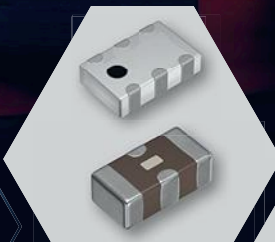
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