# Meld SDR, Host Systems, MIMO to Boost RF Comms Speed and Efficacy

High-performance software-defined-radio platforms deliver MIMO functionality and enhanced effectiveness at accelerated rates to meet advanced communication network needs.

igh-performance software-defined-radio (SDR)<br>platforms can provide the multiple-input, mul-<br>tiple-output (MIMO) functionality, increased<br>speed, and improved effectiveness demanded by<br>advanced communication networks. They a igh-performance software-defined-radio (SDR) platforms can provide the multiple-input, multiple-output (MIMO) functionality, increased speed, and improved effectiveness demanded by advanced communication networks. They also can capture speed communication links by using a powerful host system.

In addition, SDR systems offer high-quality RF performance in their signal chains, enabling advanced antenna systems. As a result, they're able to work effectively in congested environments.

This article explores various capabilities of high-performance SDR systems, how their performance is achieved, and how they benefit advanced communication networks. We discuss how MIMO communications help to enhance raw data throughput in applications where the spectral environment is limited, congested, or challenging.

Furthermore, we'll look at how the pairing of high-performance SDR and host systems helps to achieve the high bandwidth required for high-speed performance. Finally, the article discusses how the tuning range flexibility and reconfigurability of the FPGA helps enhance the overall effectiveness of advanced communication systems.

#### **SDR and Host Systems**

A typical SDR system consists of a radio front end (RFE), a mixed-signal interface, and a digital back end (DBE). To start with, the RFE features receive (Rx) and transmit (Tx) channels that provide a wide tuning range, usually tens of gigahertz. The mixed-signal interface integrates analog-todigital converters (ADCs) for the receiver chains and digital-to-analog converters (DACs) for the transmitter chains. Most high-performance SDR systems maintain fully independent Tx and Rx channels. SDR systems have additional boards for timing and power-supply functions, too.

The DBE of an SDR system features an FPGA that offers a variety of onboard digital-signal-processing (DSP) capabilities, including packetization of data, upconverting, downconverting, modulation, and demodulation. These FPGAs can support various application-specific functions, such as security schemes, channelization, and machine-learning and artificial-intelligence algorithms. Due to advanced FP-GAs and converters, the highest-bandwidth SDR systems offer instantaneous bandwidths of up to 3 GHz per channel.

FPGAs are highly suitable for tasks involving pre-processing of data, such as channelization, security schemes, and modems, before the data is sent to a host system or network server over a physical link. Communicating with host systems or network servers is accomplished by transporting Ethernet packets (containing VITA 49 protocol IQ data) over SFP+/qSFP+ links at transmission rates of 10 to 100 Gb/s.

A host system is a critical part of an SDR-based system and is connected via the SDR's Ethernet ports and MGMT ports. Apart from controlling and configuring the SDR, the host also sends, receives, captures, and monitors the raw IQ data.

Host systems used in high-speed applications feature network interface cards (NICs), central processing units (CPUs), and double-data-rate fourth-generation randomaccess memory (DDR4 RAM) chips that are optimized to enable high-speed performance. These components are combined in a server system comprising a powerful computer capable of matching the performance of an SDR. *Figure 1* shows a high-performance SDR-based system consisting of an SDR platform and a host system.



**SDR** platform

**Host system** 

1. Shown is a block diagram of a system consisting of an SDR and a host.

### **How SDRs and Host Systems Speed Data Processing**

The highly parallel architecture of an FPGA system allows for very high sampling rates and, hence, very high instantaneous bandwidths. The instantaneous bandwidth available to an SDR system is determined by the sampling rate of its ADCs, as stipulated in the Nyquist-Shannon sampling theorem. In practice, achieving very high data rates requires an FPGA platform with JESD204 interfaces.

High-performance SDR platforms utilize complex sampling devices to reach those high data rates. With a complex signal, the sampling bandwidth is equal to the sampling rate. Compared to real-valued signals, the orthogonal components of a complex signal (IQ pairs) carry double the amount of information.

One of the main benefits of utilizing complex sampling devices is that it allows for unaliased signal processing. Secondly, IQ sampling enables the use of complex modulation and demodulation schemes that have a higher capacity for information encoding. For example, QAM with a suitable constellation size makes it possible to achieve higher spectral efficiencies.

With IQ sampling, SDR platforms using 1- and 3-Gsample/s devices can attain high instantaneous sampling bandwidths of 1 to 3 GHz. Such an SDR is able to simul-

taneously observe the entire sampling bandwidth. A large instantaneous bandwidth allows for detection of interfering RF signals over a wide frequency band. In addition, simultaneous processing of different signals in wideband is possible, a technique that's commonly known as channelization.

Some of the common methods of performing channelization include frequency-domain filtering, digital downconversion, and polyphase fast-Fourier-transform (FFT) filtering. Channelization is the process of removing the unwanted portions of a signal and decreasing the sampling rate to the minimum.

For instance, if the sample rate of a signal is reduced from 100 MHz to 400 kHz, the amount of data in the signal shrinks 250X. This reduction in data size helps to save the processing power of a host system, thereby enabling faster extraction of channels using limited CPU capabilities.

The capability to extract and process many channels simultaneously from a wideband signal greatly benefits many applications, including radar, Global Navigation Satellite System (GNSS), and signal surveillance. An FPGA's parallel architecture can extract thousands of signals from a wideband input in real-time. Adding the capability to stream channels makes this feature even more attractive to advanced wireless communication applications. *Figure 2* illus-





3. Here, we show how the direction of a beam is steered by adjusting the phase of the signals in a phased-array system.

trates extraction of different signals from a wideband input using an FPGA-based channelization technique.

Channelization also enables the use of a single physical SMA port to receive different signals with different modulation schemes and decode or demodulate them simultaneously. Wideband architectures are commonly used in communication infrastructure systems that may have many carrier channels active at the same time. Examples of such communication systems include satellite communication hubs, tactical communications gateways, and cellular base stations.

As discussed, the FPGA can packetize data over 10/40/100-Gb/s Ethernet and transfer the packets to a host system. This capability is of great benefit to applications involving real-time monitoring and processing of data over large instantaneous bandwidths, such as spectrum monitoring and recording.

However, doing so requires use of a high-performance host system capable of processing huge volumes of data. Such host systems utilize FPGA-accelerated network-interface cards (NICs), redundant-array-of-independent-disks (RAID) configurations, Non-Volatile Memory Express solid-state drives (NVMe SSDs), CPUs with many cores and multithreading, and Data Plane Development Kits (DPDKs) to bypass the operating-system (OS) kernel. SDR systems with the highest data throughput are commonly used in wideband spectrum monitoring and recording, among other throughput-demanding applications.

An FPGA offers a broad array of onboard processing capabilities and can be used for pre-processing or processing IQ data as a standalone device. A variety of standalone devices such as ultra-fast modems can be realized on an FPGA. It's also possible to embed complex application logic such as cognitive-radio (CR) applications on these highly parallel devices. CR applications enable a radio system to adjust operating characteristics and transmitter parameters based on a system's interactions with its environment.

### **How SDRs and Host Systems Increase Tx/Rx Effectiveness**

A well-designed RFE is required for quality transmission and reception of signals. Utilizing a high-performance RFE simplifies processing and enhances the overall effectiveness of a radio chain. RF specifications that are significantly influenced by the quality of the RFE include mixing products/spurs, dynamic range/sensitivity, phase, gain, noise, and crosstalk. A high-performance RFE minimizes mixing products, thereby increasing the spurious-free dynamic range (SFDR) to enhance the interception of weak signals.

A high-performance RFE provides flat phase and gain, thereby helping to prevent signal distortion. Using a highquality RFE with a proper low-noise amplifier (LNA) also minimizes noise on the Rx side. In addition, a high-performance RFE helps prevent interference and crosstalk between different transmit and receive channels. Similarly, it's vital to prevent crosstalk between the RFE and the digital backend. For instance, proper isolation of different channels is important in MIMO systems to prevent such crosstalk.

MIMO configurations enable different antennas to be easily connected to an SDR's many Tx/Rx chains. As a result, signals may be retransmitted on a different frequency channel if one is jammed or congested. MIMO SDR is hugely beneficial to military and other applications in which redundancy and reliability are critical factors. Such a configuration is necessary when detecting different bands as well as for applications involving different directionalities of antenna gain.

Because MIMO channels generate huge amounts of data, high-performance FPGAs and host systems are required to process IQ samples. And, because throughput requirements intensify with an increase in the number of Tx/Rx chains, a powerful digital backhaul is a crucial component for MIMO applications.

MIMO enriches military applications by adding a variety of critical features, including reduced probability of intercept, improved anti-jamming capability, and low visibility of antennas due to reduced aperture areas. Furthermore, because no additional resources are required, MIMO enhances the overall reliability of a communication system.

MIMO also enables the use of advanced antenna techniques, such as beamforming and spatial multiplexing, to increase effectiveness of radio communications. Spatial multiplexing is an advanced technique that exploits the channel bandwidth spacing differences between transmitting and receiving antennas to provide multiple parallel streams, thereby increasing data throughput. This technique enhances spectral efficiency and benefits applications ranging from industrial Internet of Things (IIoT) to military systems and satcom.

On the other hand, transmit beamforming is a technique that enables an access point to utilize more than one antenna in a phased-array configuration. A phased-array system controls the amplitude and phase of the transmitted data to produce a directional beam. One obtains the best signalto-noise ratio (SNR), data amplitude, and range when the transmitted data's amplitude and phase are adjusted to the optimal values. *Figure 3* shows how the direction of a beam is steered by adjusting the phase of the signals in a phasedarray system.

By using an SDR that supports GNU radio, one can easily create flowgraphs for MIMO beamforming and spatial multiplexing. This open-source toolkit also can be used to develop testbeds that evaluate the performance of spatial multiplexing and other advanced communication techniques.

## **Conclusion**

SDR and host-system platforms come equipped with capabilities to implement advanced wireless communication systems that deliver improved speed and effectiveness. Reconfigurable FPGAs in SDR platforms offer a broad array of onboard DSP capabilities required to realize and test complex high-throughput systems. The RFEs and FPGAs employed in high-performance SDR systems enable implementation of various communication techniques, such as MIMO communication, channelization, beamforming, and spatial multiplexing.

Per Vices specializes in the design and development of high performance SDR platforms for use in a variety of applications, including radar, satellite communications, medical, low-latency links, test and measurement, spectrum monitoring, and mobile communications.



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