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TEST'S EVOLUTION MIRRORS THE WIRELESS WORLD

CONTENTS

There is no precision without feedback, and the increased levels of integration and complexity in wireless systems demand the latest in test & measurement tools for validation and optimization.

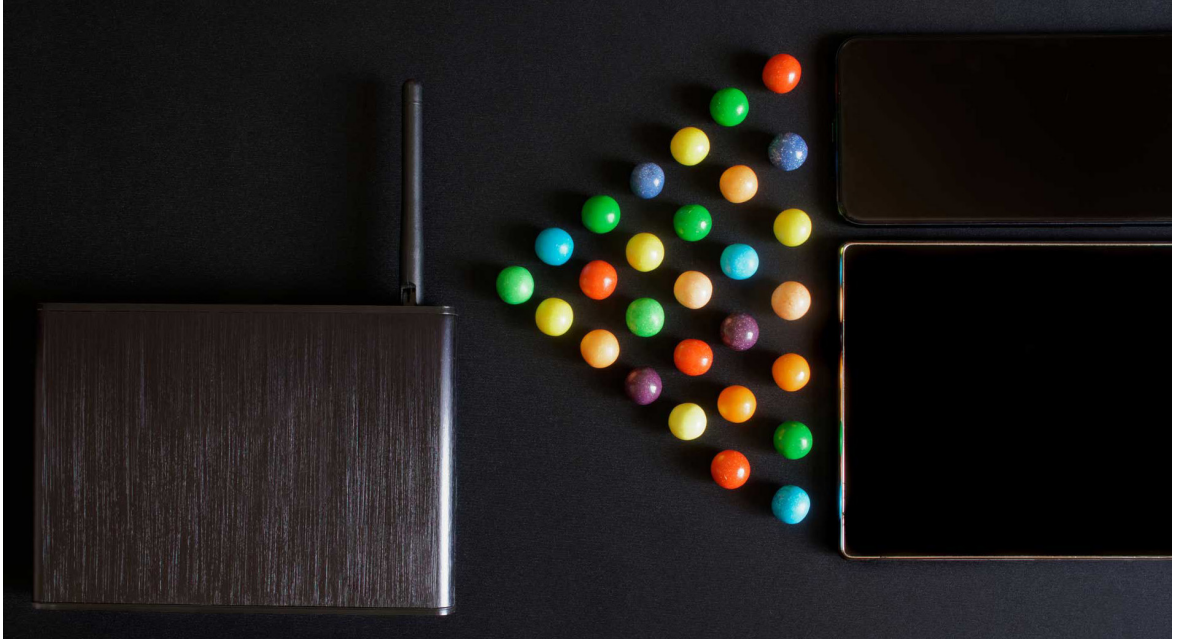
Alix Paultre
Editor-at Large
Microwaves & RF
Electronic Design

Advanced electronic devices, products, and services have transformed society at every level, from the individual to the nation-state, from business to pleasure, and from handhelds to smart-city infrastructures. These next-generation solutions are powerful and functional, but most of that advanced toolset comes from wireless connectivity. The ability to communicate with other intelligent devices around you is the foundation of the IoT.

The growth in the use of wireless Cloud-based systems and services has also resulted in a growth of the interconnected intelligent systems and their related wireless infrastructures. For every wireless entity in the Cloud, there is a corresponding amount of wiring behind the wall's wainscotting, as it were. Evey base station, modem, and endpoint is a hybrid system, with both wired and wireless aspects that must work in harmony at all times to be functional.

It is critical to ensure these solutions are not only operating in an optimum manner, but are doing so in a way that does not interfere with the other wireless systems in the field. To do so they must all be thoroughly evaluated for performance and compliance with the latest advanced test & measurement systems to address regulatory and industry requirements.

The need for faster systems that can capture large amounts of data quickly and accurately is critical, and the latest test solutions are rising to the task. This March, Microwaves & RF will explore the present and future of test and measurement, with a full week of feature articles and other content from around the industry about this important topic.



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CHAPTER 1:

VNAs Must Keep Pace with Advanced Signal-Integrity Demands

NAVNEET KATARIA, Product Marketing Manager, *Anritsu*

A vector network analyzer needs the proper frequency coverage and dedicated SI measurement tools to achieve accurate and repeatable results for today's high-speed designs.

Maintaining signal integrity (SI) in high-speed digital designs is becoming a more daunting task with the rollout of each new technology generation. As data rates reach 128 Gb/s and beyond, printed-circuit-board (PCBs) space diminishing, and system designs shrinking in size, engineers need advanced test solutions that support high frequencies.

Vector network analyzers (VNAs) have become the instrument of choice for many SI engineers. However, the analyzers must provide proper frequency coverage and have specific SI analysis tools to conduct accurate, repeatable measurements.

What Causes Signal Degradation?

Engineers conduct signal-integrity measurements to ensure the quality of an electrical signal meets designated industry standards. Signal integrity specifically addresses issues related to channels on parts such as backplanes, PCBs, connectors, cables, as well as active components in the serializer and deserializer (SerDes).

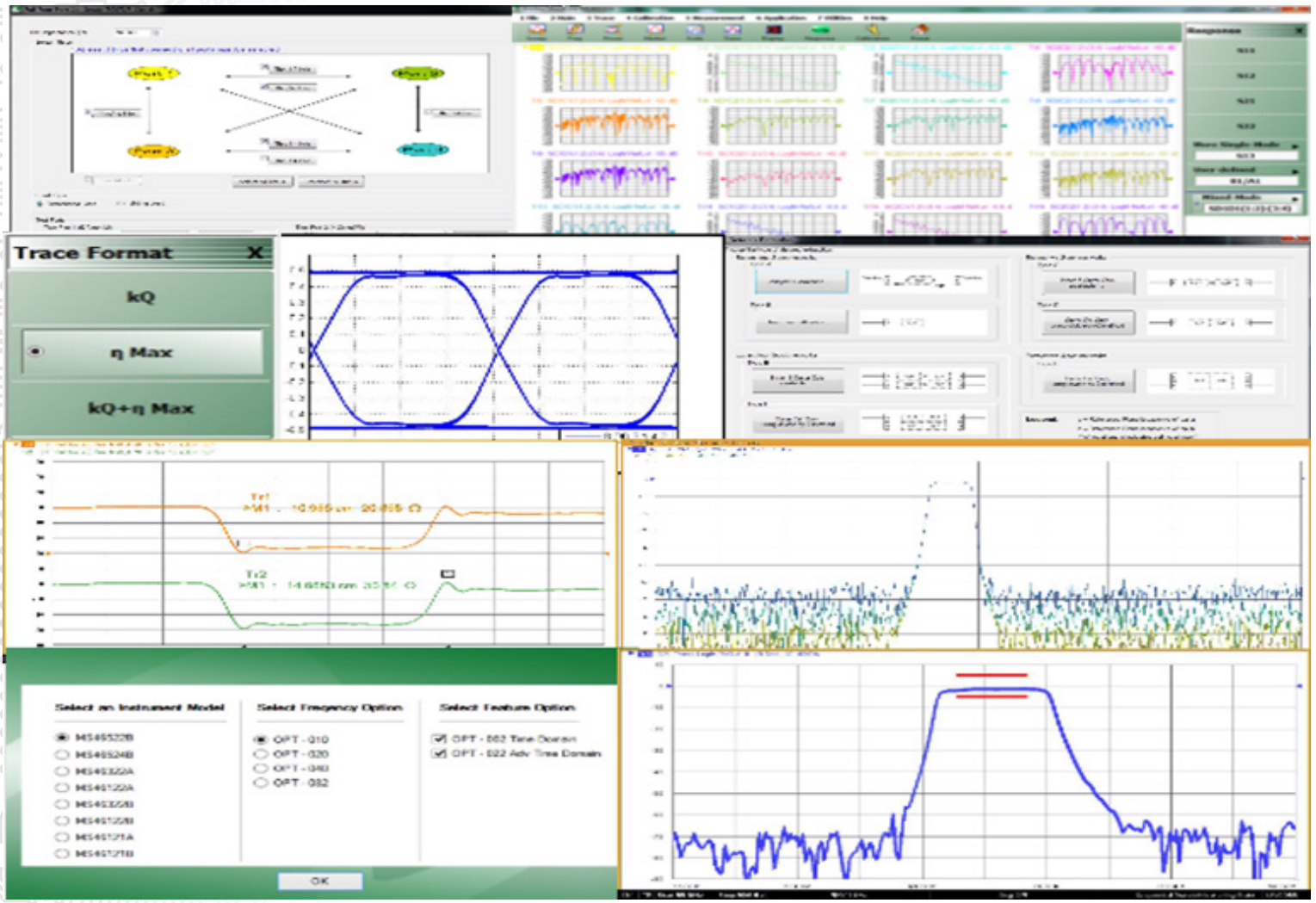
POTENTIAL FACTORS THAT DEGRADE PCB SIGNALS	
Connector construction and mounting performance	Lack of ground planes and ground vias
Imperfect vias (multilayer)	Tolerances on PCB artwork (plating and dielectric thickness variations)

Signal quality is degraded by quantities such as the loss of amplitude, crosstalk, delay, jitter, noise, and interference. Signal degradation on a PCB can be caused by a number of factors, most notably those listed in the **table**.

Benefits of VNAs in Signal-Integrity Verification

VNAs hold significant advantages over traditional time-domain-reflectometry (TDR) measurement equipment, especially as speeds ramp up. Proper SI VNAs incorporate the capabilities of TDR and impedance equipment, but they also provide improved electrostatic-discharge (ESD) protection as well as support frequency- and time-domain testing, including TDR, impedance, and Delta-L (**Fig. 1**). VNAs also allow for automatic measurements to be made to save time and improve repeatability.

Moreover, VNAs have more extensive functionality with better specifications to support differential testing for high-speed backplane applications. On top of that, certain VNAs for SI applications maintain a more flexible compact hardware architecture that includes two receivers per port in a more robust single-chassis construction.



1. VNAs for signal-integrity testing support frequency- and time-domain measurements.

Choosing the Correct VNA Frequency

When selecting a VNA for signal-integrity designs, frequency coverage is an important consideration. There's a correlation between the analyzer's frequency range and the clock rate of the signal.

For example, a 40-Gb/s system uses a 20-GHz NRZ (non-return-to-zero) clock. During development, a design engineer needs to measure the 3rd or 5th harmonic of the NRZ to characterize performance. A VNA that covers up to 40 GHz can be used to conduct measurements on the system. Measuring the 3rd harmonic of a 25-Gb/s system can be performed with a 40-GHz analyzer.

To support emerging high-speed designs, PAM4 modulation replaces NRZ. One advantage of PAM4 is that it doubles the bit rate for a given baud rate compared to NRZ. The tradeoff is the signal-to-noise (SNR) ratio is higher, making the signal much more sensitive to noise.

To support 112-Gb/s PAM4, the VNA frequency must extend to 43.5 GHz, and for a 224-Gb/s PAM4 signal, a VNA with frequency coverage up to 70 GHz is necessary. Equally important is the lower-end frequency of the VNA, as it can significantly improve modeling. For example, a 70-kHz start frequency reduces the risk of DC extrapolation errors for more accurate models. The result is fewer design turns, improving time and cost efficiencies.

VNA Tools for Signal Integrity

VNAs also need to provide specific test capabilities for SI designs. At a minimum, the VNA must support TDR-like measurements, so that the analyzer can accurately identify impedance discontinuities and other faults in data transmission cables, backplanes, and other devices under test (DUTs).

Dedicated software for network extraction and embedding/de-embedding are also valuable analysis tools for SI designs. Network extraction identifies and removes subsets of a structure, such as a test fixture, PCB, and other interconnects that behave as localized pseudo-lumped-element reflection centers.

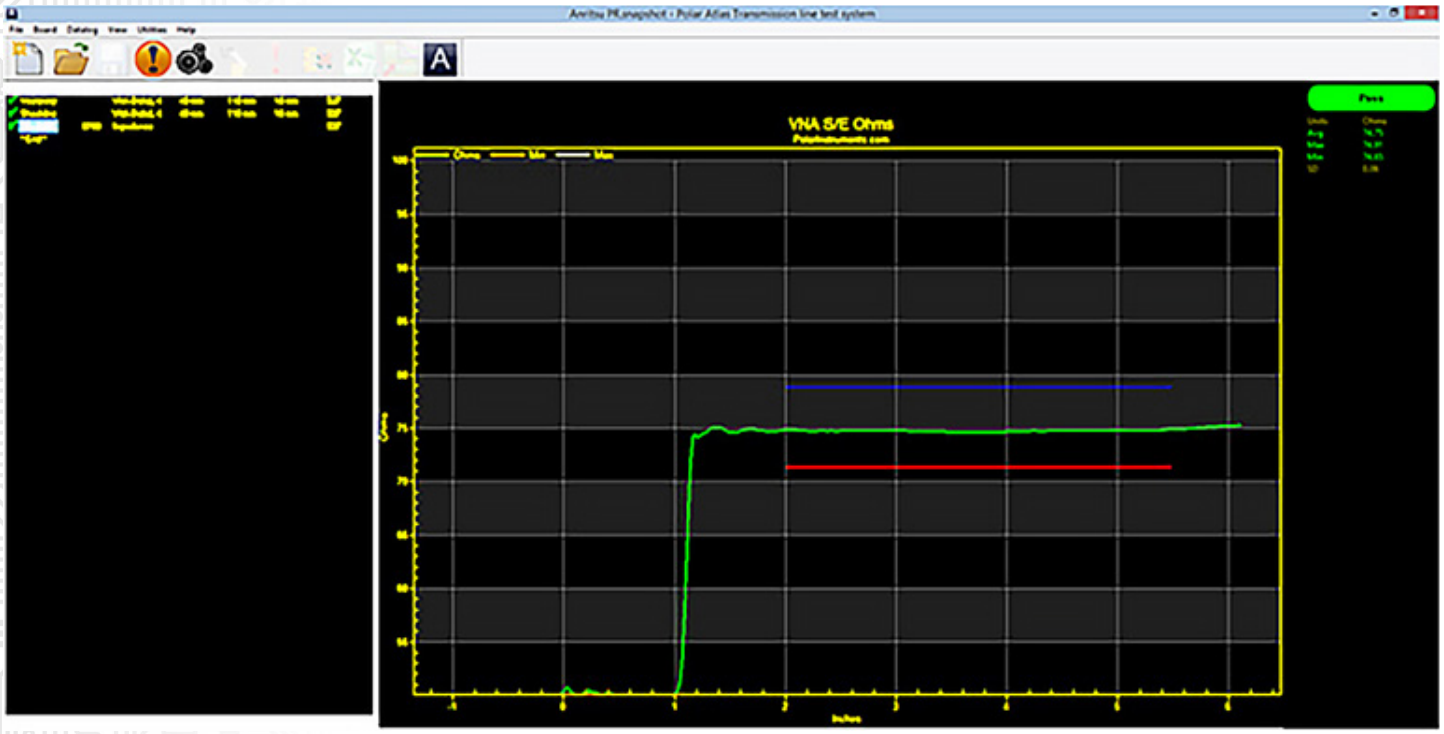
Sequential peeling is a model/measurement-based method of network extraction for de-embedding that helps analyze isolated defects within a test fixture or other complex network. The sequential-peeling technique acquires detailed information about the fixture, making it easy to improve the test fixture design and, ultimately, first-time yields.

Sequential peeling is particularly useful for electrically small structures with isolated vias in the transmission-line runs, such as on PCBs. That's because sequential peeling identifies time domain elements and then fits a shunt admittance or series impedance model to the isolated data. Once a series of these elements are identified, a more complete composite model of the structure can be obtained and de-embedded.

Delta-L Solves PCB Test Issue

Developing dedicated software that supports Delta-L enables VNAs to efficiently verify high-speed designs. Delta-L is an algorithm developed by Intel, whereby PCB manufacturers can validate their products. The VNA serves as an important requirement for all PCB makers to comply with Delta-L testing and satisfy the link budget for backplane design on Intel servers.

The key benefit of Delta-L is that it removes the effects of probes and via holes by measuring two different lengths, simplifying and improving the accuracy of acquiring PCB



2. An impedance measurement from a VNA with Delta-L software installed is leveraged to ensure PCB compliance.

characteristics. When the Delta-L software is installed, the VNA can measure insertion loss within differential pairs, and uncertainty of insertion loss, impedance, and effective dielectric constant for PCBs (**Fig. 2**).

Insertion loss is a key measurement, especially in emerging high-frequency designs. The higher the frequency, the greater the losses. When the insertion loss falls below the specified threshold, the signal is lost.

Conclusion

As high-speed designs incorporate next-generation technologies, VNAs will continue to serve as a key tool during verification. For engineers to have confidence in their high-speed designs, selecting an analyzer that has the proper frequency coverage and dedicated SI measurement tools are necessary for accurate and repeatable results that will save time and money.

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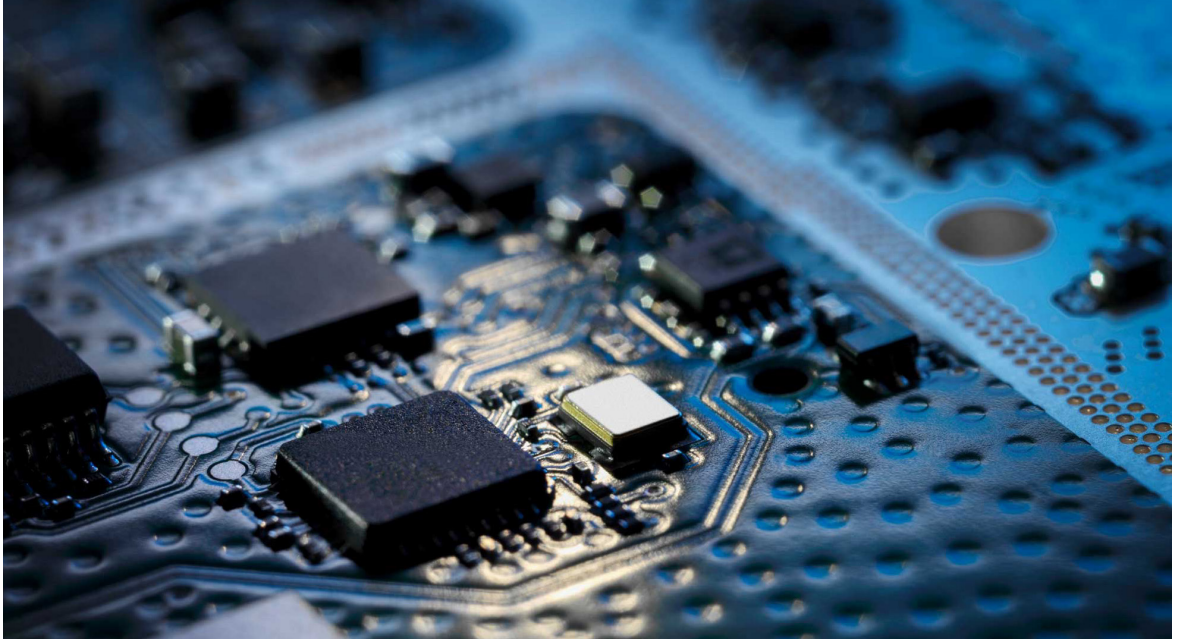


CHAPTER 2:

Optimizing RF Power Amplifiers for Wideband Comms Apps

MARKUS LÖRNER, Market Segment Manager RF & Microwave Components, *Rohde & Schwarz*, www.rohde-schwarz.com

Designing RF power amplifiers that exhibit linear behavior over a wide bandwidth and can support high-order modulation schemes becomes increasingly important as more complex, higher-data-rate wireless standards are released.

A variety of metrics, techniques, and test instruments are used to characterize RF power amplifiers to identify specific issues and optimize their performance. Communication standards are constantly evolving to support new use cases, services, and applications, each with its own set of system performance requirements. For data-intensive services, the maximum data rate able to be supported by the communication channel is of prime importance. This poses stronger requirements for the performance of active components such as RF power amplifiers.

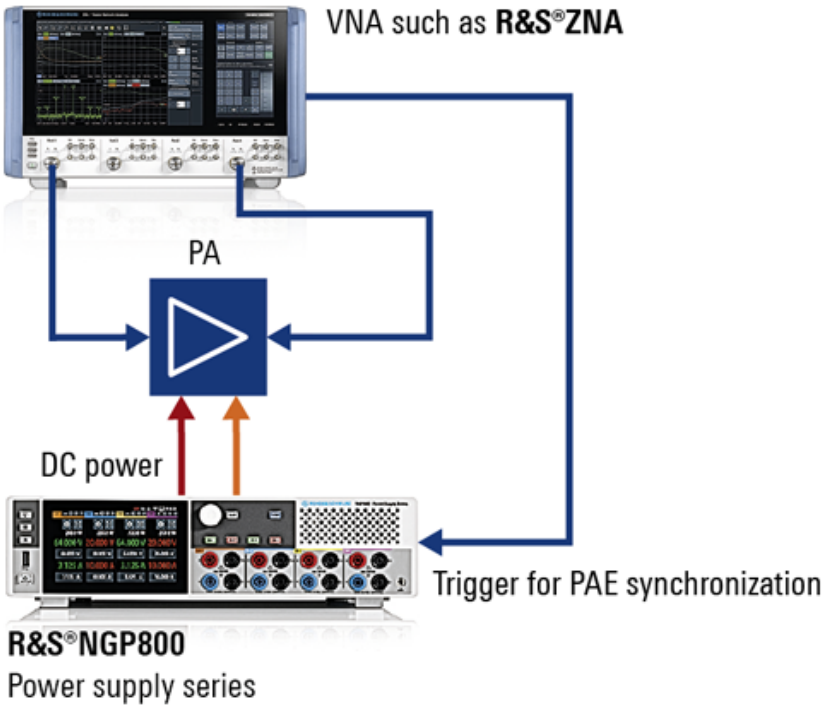
Wider channel bandwidths and higher-order digital modulation schemes offer the possibility to increase throughput, but they bring more demanding design requirements. Wider bandwidth and higher-order modulation schemes are more vulnerable to incorrectly decoded symbols and subsequent bit errors. Addressing these issues requires linear operation of the amplifier over an increased frequency range.

Basic RF Amplifier Tests

For the design engineer optimizing the behavior of amplifiers over the frequency and power range of operation, the ability to support higher-order modulated signals becomes the focus. This requires a comprehensive and well-structured test approach.

RF power-amplifier design and verification testing break down into two broad types: measuring the fundamental characteristics of an amplifier using continuous-wave (CW) signals on the one hand, then ensuring its performance under the demanding conditions of wideband, modulated signals on the other.

CW-based tests range from measuring the gain and impedance match over the frequency of operation to an understanding of the distortion introduced when it's driven



1. This setup for continuous-wave (CW) tests involves a VNA and power supply.

into nonlinear behavior, for example, compression, harmonics, and intermodulation. These tests, as well as the noise figure, efficiency, and power-added efficiency (PAE) can all be conducted using an appropriate vector network analyzer (VNA) such as the R&S ZNA together with a power supply (**Fig. 1**).

Measurement of compression points is used to understand the amplifier's useful power range before it becomes significantly nonlinear and approaches saturation. Typically, power versus gain is measured using a VNA and the 1- or 3-dB compression point is determined. Evaluating the efficiency is achieved by measuring the power supply's power consumption and comparing this with the additional RF power delivered by the output of the amplifier.

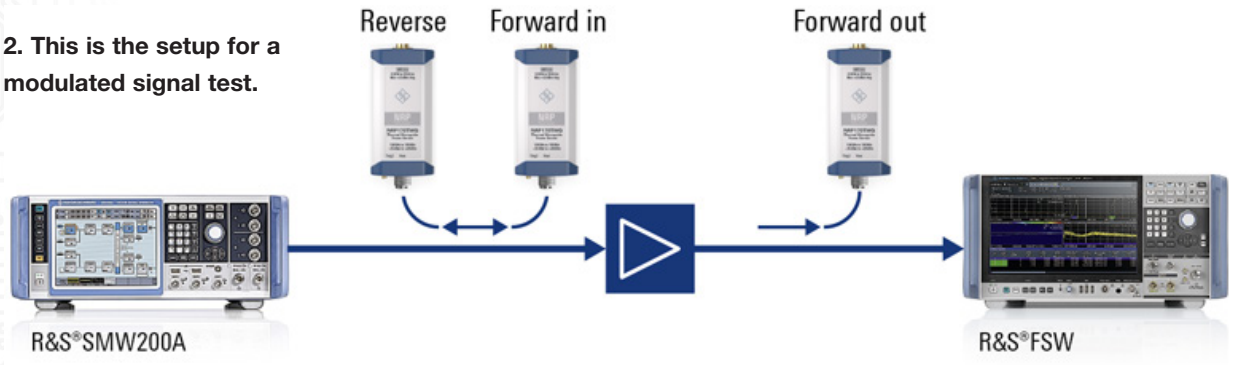
PAE evaluates the efficiency of an amplifier in terms of how effectively it adds power to an RF signal. It can be determined by using a VNA to measure input and output RF power, and a power supply to measure how much electrical power is consumed by the amplifier.

Another important indicator of nonlinearity involves the frequency components introduced by an amplifier due to intermodulation and harmonic distortion. To conduct the intermodulation test, two signals at a specific offset and power levels are fed into an amplifier and the second- and third-order intermodulation products are measured. They're then compared with the fundamental frequency signals to calculate IM2 and IM3.

Harmonic distortion is measured by running a CW signal into the power amplifier and measuring its output at multiples of the fundamental frequency. The frequency-conversion measurement capability of the VNA can be used since the harmonics are 2X, 3X, 4X, etc., of the frequency of the original input frequency.

Also vital in understanding the linearity of the amplifier is the third-order intercept point (IP3). It's a mathematical approximation of the comparison between the linear behavior and how fast the third-order harmonic is increasing.

Noise figure results in a reduced dynamic range, and a reduced signal-to-noise ratio



2. This is the setup for a modulated signal test.

(SNR) is an indication of the noise added by the amplifier itself. To measure the noise figure, the output noise versus the input noise is evaluated with the device's gain. The cold-source method employs a VNA as a source and measurement receiver; it measures noise while the source is turned off and gain while the source on.

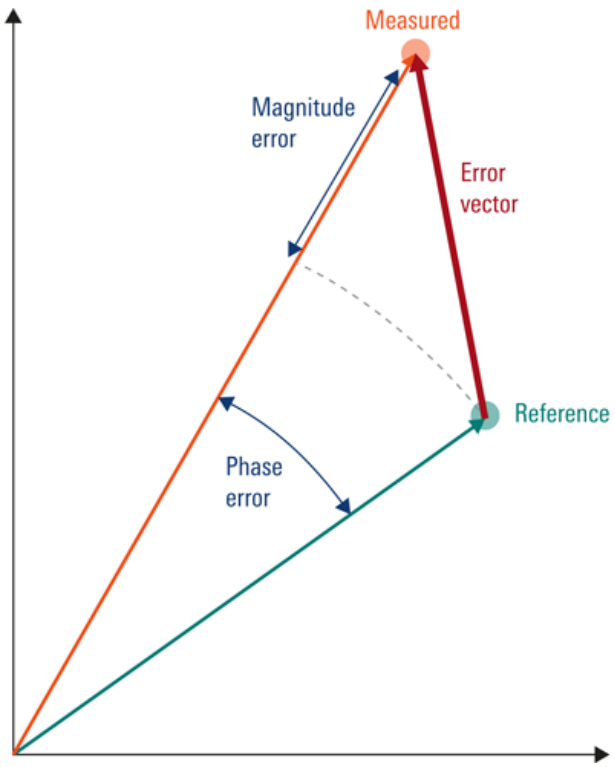
Alternatively, the Y-factor method uses a spectrum analyzer and a noise source. Two measurements are conducted: one with the noise source turned on and one with the noise source turned off. Plotting the two results, a line is taken through the measured points to derive the noise added by the amplifier alone.

From CW to Modulated Testing

Using a VNA to conduct continuous-wave testing can provide a lot of information about the amplifier's overall performance. However, modulation-based testing lets us see how the device will perform using the specific wireless standard it's intended for, such as 5G or Wi-Fi. For these types of tests, we need a vector signal generator (VSG) and a spectrum analyzer with appropriate frequency coverage and bandwidth (**Fig. 2**).

In modulation-based testing, the most important metric to characterize modulation quality is error vector magnitude (EVM). Each symbol in an I/Q constellation has an ideal or reference point that corresponds to a defined magnitude and phase, but received or measured points rarely fall exactly on the ideal point. Some of the differences are due to magnitude error and others due to phase error.

We can quantify these two sources of error by drawing a vector that connects the reference and measured points, referred to as the "error vector" (**Fig. 3**). The root



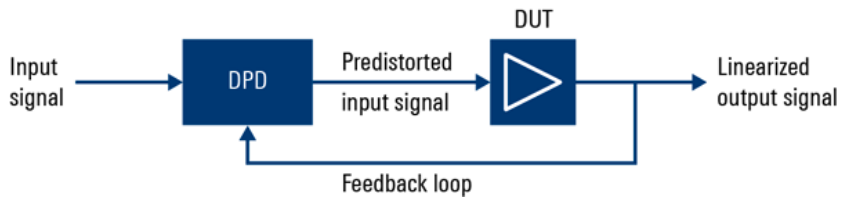
3. Calculation for error vector magnitude (EVM).

mean square (RMS) average amplitude of the error vector, normalized to ideal signal amplitude reference, is the EVM, expressed either as a percentage or in decibels. EVM is measured at each symbol time. Larger values of EVM mean a higher probability that the receiver will mistake one symbol for another, resulting in bit errors.

Measured I/Q points can be visualized in an I/Q diagram and compared with their ideal values using a constellation diagram on a spectrum analyzer. This is a very useful tool for the amplifier designer because it gives insight into the overall modulation quality. Furthermore, how the errors are distributed is indicative of specific issues with the amplifier performance, such as phase noise, random noise, or compression.

Linearization Approaches

Amplifier linearization can be done in various ways. The most common approach is to use digital predistortion (DPD) of the signal (**Fig. 4**), where the incoming waveform is modified on the fly in a device implementation to compensate for the nonlinear behavior of the power amplifier. It helps to improve signal quality and reduce EVM, while minimizing the adjacent channel leakage ratio when utilizing multiples of the signal bandwidth.



4. Shown is a simplified version of a digital predistortion (DPD) system.

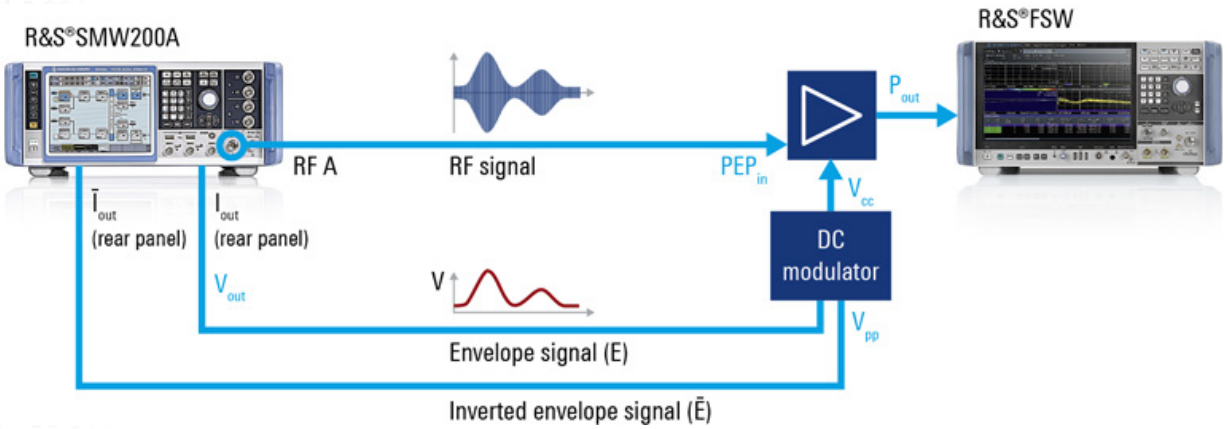
DPD, which uses mathematical algorithms, can be realized in several ways. A test-instrument assisted approach to develop DPD can deliver fast results with a straightforward process flow, offering an easy way to understand an amplifier's optimum performance with DPD. As RF PA designers, we want to understand how well we can linearize its behavior with predistortion and operate an amplifier close to compression where efficiency is highest.

The measurements required to create a model of the power amplifier can be done efficiently using the R&S SMW200A VSG with the R&S FSW signal and spectrum analyzer. The internal waveform-generation capabilities of the signal generator create various standard-compliant test signals, such as 5G. The analyzer performs all characterization measurements required for any test signal from a single data acquisition. The input signal is manipulated in an iterative process to achieve the best result for a given operating point.

The FSW analyzer allows for two DPD modes—the real-time polynomial approach, which fits the needs for mobile devices, and Direct DPD, which provides ideal predistortion, including memory effect, by correcting the signal on a sample-by-sample basis.

Efficiency Enhancements

Envelope tracking (ET) is a very common optimization technique employed in designs of battery-powered devices like mobile phones. A combination of VSG and spectrum analyzer (**Fig. 5**) form a simple but powerful test setup for ET applications. The ET technique avoids wasted energy being dissipated as heat and maximizes the battery life, making the device much more efficient.

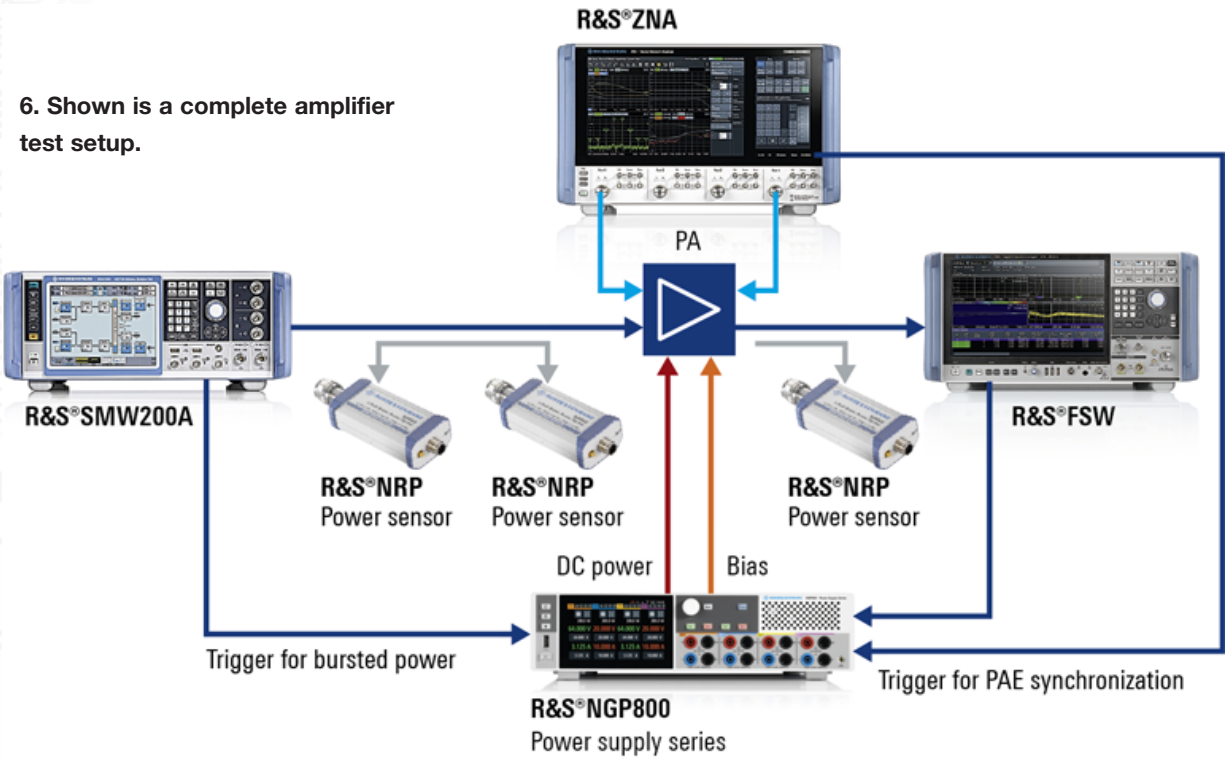


5. A combination of vector signal generator and spectrum analyzer are used in the test setup for envelope tracking.

The crest factor describes the ratio between the peak and the average power in the signal. Some high-power peaks are statistically extremely rare. However, to transmit the whole signal linearly, they need to be kept within the linear range of the amplifier. These high peaks can create intermodulation, but when the signal into the amplifier is modified by cutting off rare peaks, the effect on the signal content is minimal. In addition, the complete remaining signal can be shifted closer toward the maximum linear range of the device.

Integrated Test Setup

Combining the instruments of the CW and modulated signal tests to create an integrated amplifier test stand (**Fig. 6**) not only provides complete test coverage with the required flexibility and accuracy, but also enables synchronized measurements. Furthermore, having one connection to the DUT for all tests allows for faster and smoother testing without re-cabling.



6. Shown is a complete amplifier test setup.

In summary, high-throughput wireless communications systems require higher-order modulation schemes to increase the number of bits per symbol in a given bandwidth, causing the symbols to be closer together. This, in turn, requires higher modulation and demodulation accuracy to avoid bit errors.

EVM is the primary key performance indicator (KPI) of modulation quality. Deriving and analyzing EVM to understand the cause of signal imperfections is an essential tool for RF power-amplifier designers.

A combination of CW and modulation testing are applied for complete evaluation of designs during the development, validation, and production of RF power amplifiers. The process can be structured by first conducting fundamental characterization of the amplifier using CW techniques, using modulated signals for wireless standard-specific testing, and then implementing linearization in a particular DPD.

This can be achieved very efficiently with a surprisingly simple test setup consisting of a VNA, VSG, signal analyzer, and power supply. It provides the designer with a complete solution for developing amplifiers that can operate over wide bandwidths using higher-order modulation signals.

References

"Testing RF power amplifier designs," Rohde & Schwarz GmbH & Co. KG, PD 3608.0391.92, Version 01.00, November 2023.

"RF amplifier testing -from wafer to design-in," Rohde & Schwarz, PD 5215.7568.32, Version 02.02, April 2023.

"Understanding EVM," Paul Dominowski, Rohde & Schwarz GmbH & Co. KG, PD 3683.8038.52, Version 01.00, October 2022.

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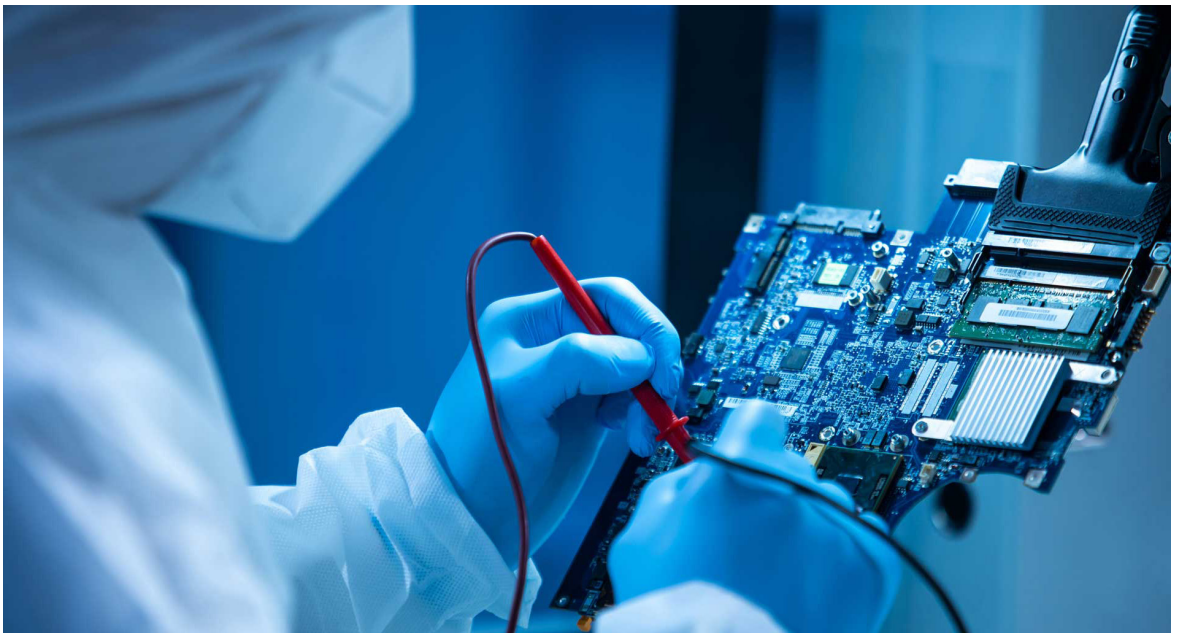

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CHAPTER 3:

The Expanding Role of Test in Advanced Electronic Systems Development

ALIX PAULTRE, Editor-at-Large

The increasing levels of functionality, integration, and networking in today's advanced electronic products brings increased attention and importance to the test & measurement technologies used in their development.

A state of disruptive evolution in embedded electronics has been a global phenomenon over the last couple of decades, with society moving from black-and-white television and AM/FM radio to AI-empowered edge computing for cloud-based applications in a single person's lifetime. This tumultuous and paradigm-changing migration to intelligent systems everywhere has changed society on every level, and there's no indication that it will slow down in terms of pace or scope anytime soon.

These sophisticated devices, products, and services, along with their related hardware and software infrastructures, place a great deal of pressure on the electronic design engineering community to create, field, and maintain them in an effective and cost-efficient manner. One of the most important tools in the engineer's bag to address these demands for optimal design is the ever-expanding capabilities in test & measurement systems and solutions.

The Importance of Test in Electronics

There's no precision without feedback, and that goes double for advanced electronic systems. Issues like power and signal management have design issues measured to multiple decimal places today, with little or no room for error. Complicating the situation, the issues of performance and precision become even more critical when considering industry standards and regional regulatory requirements.

These myriad design and compliance issues can only be addressed by testing the components, boards, devices, and systems in every electronic product, from conception to its end of warranty in the field. The test & measurement systems must not only be as

good as the electronics they're evaluating, they also must be better, operating at a faster rate and with a higher precision than their targets.

The engineer needs the largest capture at the highest rate as fast as possible to get optimal results. The the lines on your ruler must be closer together than the lines on their ruler, otherwise you can't make an accurate and useful measurement.

The need for test & measurement in advanced systems continues to evolve, with new fields of interest arriving on the scene and others leaving. The hot application spaces today aren't the same as they were 20 years ago, and the solutions being created use the latest core technologies to address them. Recently, *Microwaves & RF* conducted a short survey on what the engineering community thought would be the hot test & measurement trends of the coming year.

2024 Test & Measurement Survey Results

The Quick Poll conducted by *Microwaves & RF* simply asked the readership what they thought would be the hottest test & measurement topic in 2024. The answers covered system-level test, AI and ML verification, high-speed I/O interfaces, ATE and manufacturing test, and cybersecurity. The responses were interesting and informative (**see figure**).

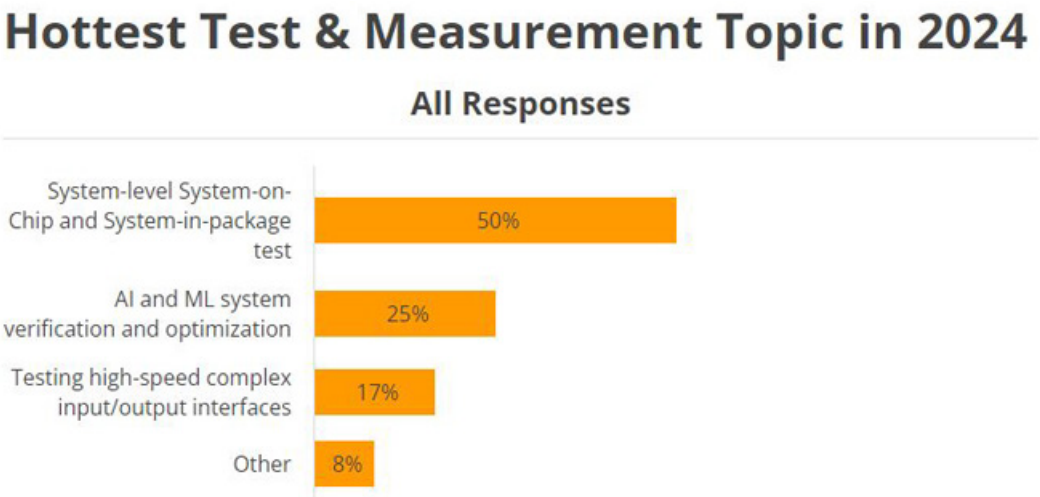

Figure 1: The responses provided by Microwaves & RF's Quick Poll were interesting and informative.

The answer "System-level System-on-Chip and System-in-package test" was the most popular response, reflecting the growing level of device integration in the industry. The increased implementation of SoC, SiP, microboard, and other highly integrated circuit topologies intensifies the system design and troubleshooting burden on the T&M industry to create tools precise and accurate enough to properly evaluate the busy data and power buses involved.

This is related to the ever-higher power densities in circuit topologies enabled by wide-bandgap semiconductors and advanced control software. Moreover, these advanced systems have to be tested for design optimization—the test tools involved must not only be fast and accurate, but also capable of handling high power peaks and transients. That challenge is compounded by the higher and higher switching speeds achieved by advanced power electronics in gallium-nitride (GaN)-based topologies.

The explosive growth of artificial-intelligence and machine-learning (AI/ML) systems and their adoption in more products and solutions demand proper verification and optimization to reach their application goals in an efficient and cost-effective manner. These test tools ironically will include their own AI/ML algorithms and protocols, which must also be verified and calibrated.

One of the bigger issues that's often ignored is the trust gap between what's generated by AI and how comfortable a person can feel using it. Proper validation and certification of AI-based solutions will go a long way toward market acceptance.

Testing high-speed complex I/O interfaces is related to the increasing level of integration and complexity in embedded systems, but it also involves the network and server infrastructure of cloud-based systems and their devices. These IoT solutions may be relatively simple at the device level, but they involve high-bandwidth data-heavy communication links to the internet via both wired and wireless technology. A complex system may have relatively simple nodes, but with a high level of network complexity.

This web of interconnectivity, from the board level to the cloud, puts added pressure on the test & measurement community—not only to create solutions that can evaluate an individual device's performance in a busy signal environment, but also how that device can impact the environment it operates in. These test tools must be able to address issues from managing board parasitics and their impact on the power and data buses on the board to how a wireless device functions in a noisy and crowded RF ecosystem.

ATE and manufacturing test didn't get enough answers to move the needle. It's a reflection of the maturity in the space and the fact that the disruptions in the industry deal with sub-categories within this space and not the space itself. There's a lot of action going on in ATE and manufacturing test, but the challenges are coming from the sectors mentioned earlier. This is also true when it comes to testing for cybersecurity compliance and immunity, as the recognition of the issues in that space comes more from adoption and awareness.

Conclusion

This year will be full of interesting technological developments, at both the scientific and applied engineering levels. Some of these developments will ramp up the challenges and opportunities in these trend areas. However, others may create new areas of interest on their own and possibly leapfrog and supersede existing issues we used to think were problems until this particular solution came along. No matter the situation, though, and no matter what next big trend(s) unfold, they will have to be tested and evaluated for performance, compliance, safety, and functionality.

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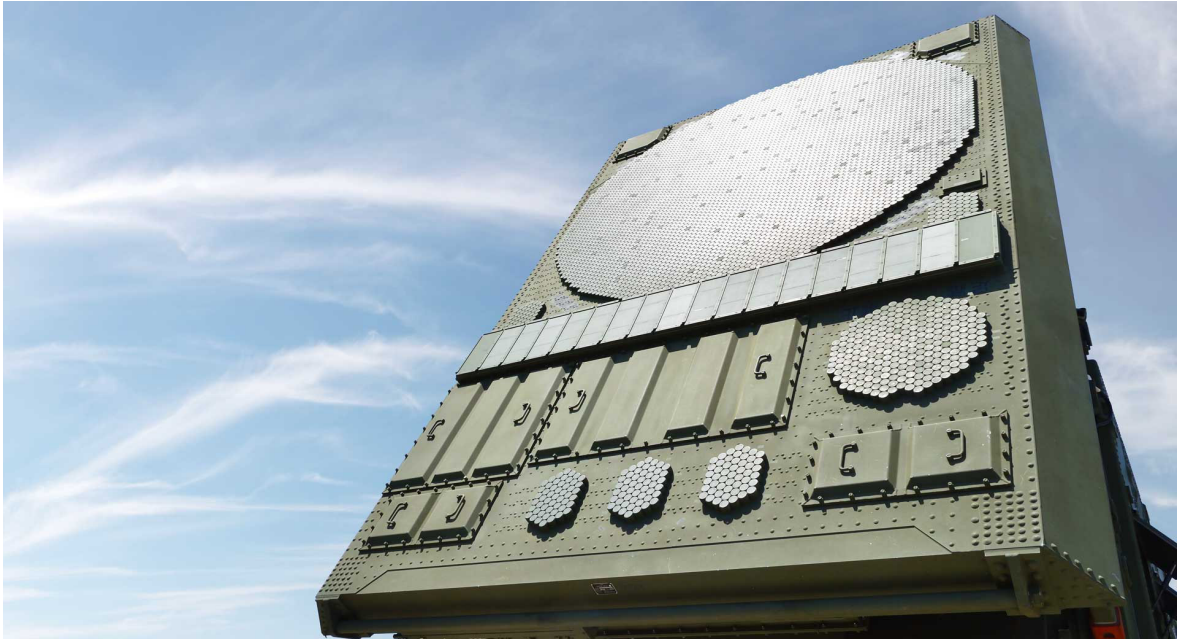


Image: AESA

CHAPTER 4:

Customizing Tests for Today's Electronically Scanned Arrays

MIKE BARRICK, Business Dev Manager, *NI*

The first scanned phased arrays used a single transmitter and receiver connected to all antenna elements through phase shifters. Currently, most use solid-state transmit/receive modules.

The first scanned phased arrays used a single transmitter and receiver connected to all antenna elements through phase shifters. Today's active electronically scanned arrays (AESAs) employ many solid-state transmit/receive modules (TRMs), each connected to an antenna element.

Rearchitecting the AESA with TRMs was made possible by advances in semiconductor technology during the 1980s, including MESFETs and JFETs for transmit power amplification, and gallium arsenide (GaAs) for low-noise receive amplification. Size, cost, and power consumption of TRMs have been reduced over time, creating potential for future commercial applications.

Radar Beamwidth vs. Array Size and Number of TRMs

One of the primary factors affecting radar system performance is the beamwidth of the antenna. Assuming the antenna element used with a TRM is a half-wave dipole, this would spread the transmitted energy over a 78-degree beamwidth, with similar performance on receive.

While that might be acceptable for gross detection of aircraft or other objects, such broad beamwidth would mean that radar returns are received from a wide range of "targets'' and "clutter" within the beamwidth, including undesired aircraft, foliage, and other elements. Narrower beamwidths would be more beneficial for higher performance.

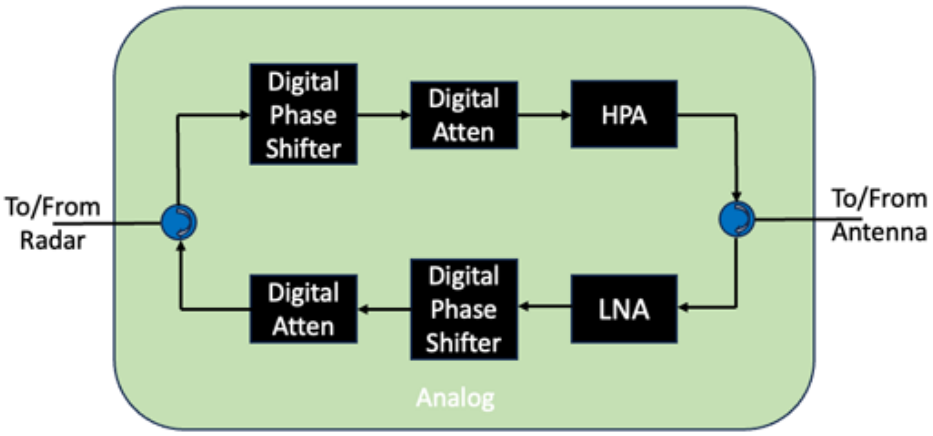
Increasing the AESA size by using more TRMs simultaneously achieves narrower beamwidth and higher gain. Beamwidth is inversely proportional to array size, while gain is directly proportional to array size.

As a result, larger arrays with increasing numbers of TRMs would provide higher performance with the ability to pick out single targets at longer range and reject the effects of clutter. Although large arrays may be desired for increased radar performance, it's easy

to see that there are limitations on size due to limited available "real estate," as well as total cost for multiple TRMs (including test).

Definition and Types of TRMs

- A TRM provides a range of functionality in a radar system:
- High power amplification (HPA) for the transmitter
- Low-noise amplification (LNA) for the receiver
- Digitally controlled phase shifting
- Digitally controlled attenuators to set power levels in the TRM



1. Shown is a block diagram of an analog TRM.

Figure 1 shows a high-level block diagram of an analog TRM. Newer digital TRMs (DTRMs) receive digital data from the radar system and convert back to digital on the receive side. Often, this leverages newer "Direct Sampling" techniques to convert received RF to digital as close to the antenna as possible, enabling radar processing in the DTRM.

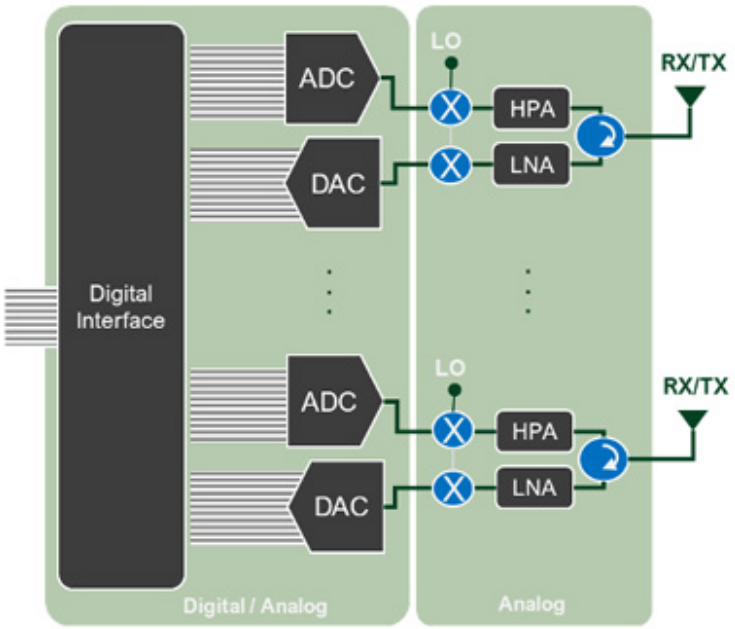
A high-level block diagram of two DTRMs with antennas is illustrated in **Figure 2**. AESAs configured with DTRMs offer advantages such as reduction of module weight and size due to increased digital vs. analog content. However, the evolution to DTRMs also presents new challenges. Foremost among them is how to test DTRMs from "RF to bits" in development, verification, and production test phases.

What's Required to Test a TRM?

Since their inception, analog TRMs have been tested using systems of vector network analyzers (VNAs), vector signal generators (VSGs), and vector signal analyzers (VSAs). Depending on the stage in the DTRM development/verification/production cycle, each of these instruments can be used to extract different and varying levels of measurement data to support test objectives.

VNAs fundamentally provide small signal S-parameter measurements such as gain, input match, and output match, and enable calibration of the TRM using a range of transmit and receive gain and phase settings. In addition to CW measurements, some VNAs can be useful for pulsed measurements, enabling measurement of semiconductor devices in the power amplifier that are unable to operate at 100% duty cycle.

2. Here, two DTRMs are employed in an AESA.



The pairing of VSG with VNA provides added measurement capability that will be required for some stages of testing. These instruments allow the test engineer to excite the TRM with a customizable waveform and measure the signal on the output. A wide range of potential measurements are enabled using these instruments, including noise figure (NF), adjacent channel power (ACP), error vector magnitude (EVM), third-order intercept (TOI), power-added efficiency (PAE), and others.

As described in the previous section, DTRMs no longer have an analog input/output for testing, so traditional instruments have limited utility. New solutions matching the mixed-signal nature of DTRMs are required, with capability to make new measurements that are analogous to VNAs, VSGs, and VSAs.

New Measurements for DTRMs

The major change in the transition from analog TRMs to DTRMs is replacement of the RF port from the radar with a digital serial and/or parallel port. Measurements similar to traditional measurements are still required, but new means of emulating digital signals from the radar are needed. While traditional VNA RF in/RF out measurements no longer exist for DTRMs, analogous measurements with Digital in/RF out and RF in/Digital out are now possible.

Assuming that digital data is supplied to the DTRM to activate a specific RF frequency/phase/amplitude output and sequenced to the next RF state, it's possible to construct swept measurements similar to VNA S21 measurements. Likewise, assuming that RF at a specific RF state is supplied to the DTRM and sequenced to the next RF state, swept measurements akin to VNA S12 measurements are possible. If desired, output match (S22) could also be measured using traditional RF techniques.

Traditional VSG/VSA measurements could be emulated using similar techniques. Analogs to traditional TX measurements such as Power, ACP, EVM, TOI, PAE, and others could be constructed using the appropriate digital data into the DTRM and measuring RF with a VSA. Likewise, analogs to traditional RX measurements such as BER/BLER and

NF could be constructed using the appropriate RF state and data stream into the DTRM and measuring data on the digital side.

The Value of PXI for DTRM Test

Today's modular measurement solutions enable the user to configure multifunction instruments in a single chassis, matching the mixed-signal Digital+RF requirements for DTRMs. A combination of serial and parallel data modules along with RF modules meets unique test requirements for the mixed-signal digital/RF nature of the DTRM. When paired with CW and pulsed power-supply modules, the result is a compact solution offering a unique set of measurements fitting DTRM test requirements.

PCI eXtensions for Instrumentation (PXI) is the leading modular measurement solution in the market, and a wide range of modules matching DTRM test needs are available. National Instruments (now NI, an Emerson company) founded PXI in 1997, and has developed a wide range of modular instruments matching industry requirements since that time. Relative to DTRM test requirements, this includes:

- Vector signal transceiver (VST) modules combining both VSG and VSA functionality in a small form factor.
- VNA modules, including the newest version that enables combined VST and VNA measurements on a single set of ports.
- Source measurement unit (SMU) modules to provide CW and pulsed power to the system under test (SUT).
- Tight timing synchronization of all modules in the chassis using the PXI backplane.

For example, the new PXIe-5842 VST instrument is capable of RF measurements from

3. Capable of RF measurements from 30 MHz to 26.5/54 GHz, the PXIe-5842 VST has options for 2 and 4 GHz of instantaneous bandwidth.

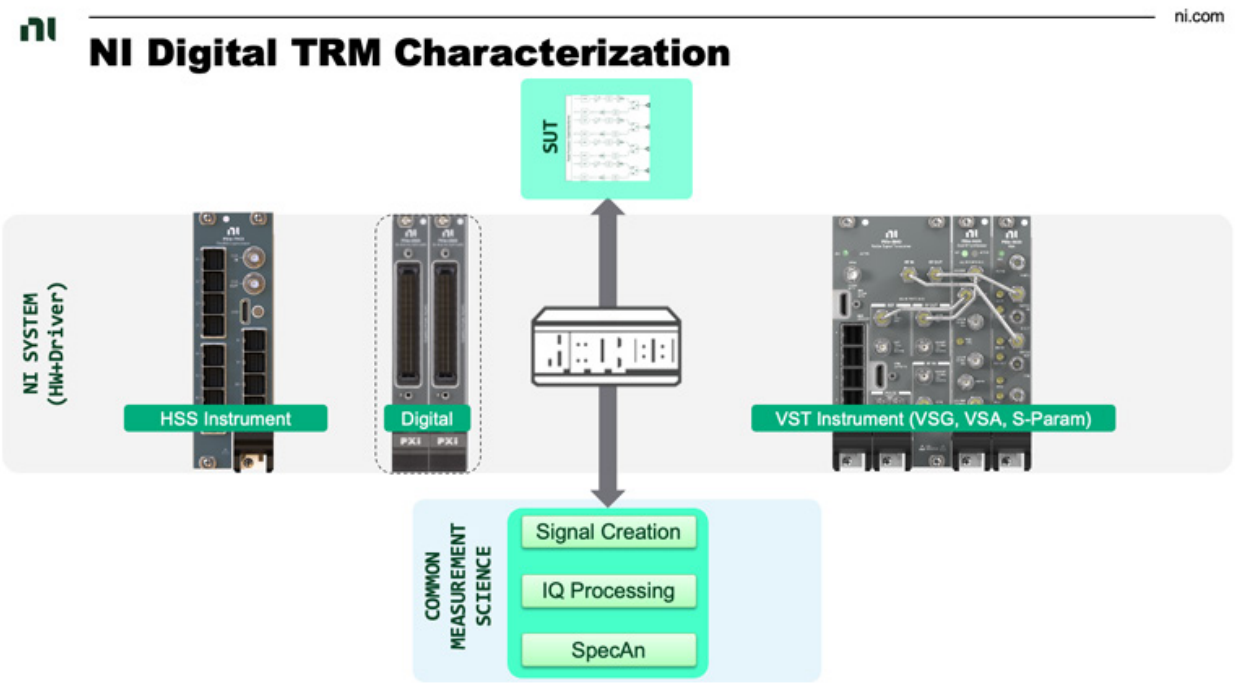
PXIe-5842 | 26.5 GHz VST

- Extended contiguous frequency coverage (mmWave extension up to 54 GHz)
- Wide instantaneous bandwidth
- Best-in-class EVM performance
- Expand Capabilities with Flexible Licensing/Upgrade Options (S-parameter add-on module)
- Future path for 4 GHz BW with External Co-processor
- Common SW tools to PXIe-583x and PXIe-5841

Parameter	Instrument Capability
Frequency Range	30 MHz – 26.5 GHz
Bandwidth	Up to 2 GHz Up to 4 GHz (limited functionality)**
RF IN / OUT Flatness (2 GHz)	< ±0.45 dB typ. / < ±0.4 dB typ.
RF IN / OUT Absolute Accuracy	< ±0.4 dB typ.
Max Unleveled Tx Power	+25 dBm typ. (<18 GHz)
802.11be, 320 MHz EVM	Better than -52 dB (noise comp enabled)

*Upgrade from 23 GHz HW to 26.5 GHz HW requires a paid upgrade service
** With Limited Functionality

EMERSON



4. This single-chassis solution fits complex measurement requirements for mixed signal digital/RF DTRMs.

30 MHz to 26.5/54 GHz. Options for 2 and 4 GHz of instantaneous bandwidth (IBW) exceed typical bandwidths used for modern radars. Measurement algorithms are available to accelerate implementation of customizable measurements, including NF, ACP, EVM, TOI, PAE, and other parameters (**Fig. 3**). Optional addition of the PXIe-5633 module enables measurement of DTRM output match (S22) as needed.

When paired with additional NI PXI modules for high-speed serial (HSS), digital control, and power supply, a single-chassis solution can be assembled that fits complex measurement requirements for mixed-signal digital/RF DTRMs (**Fig. 4**).

Conclusion

Modern AESA-based radars use numerous TRMs to achieve high performance with narrow beamwidths and high gain. Each of the TRMs in the AESA must be tested in development, verification, and production to verify performance in design and guarantee performance on the battlefield.

Test solutions for legacy analog TRMs have consisted of VNAs, VSGs, and VSAs, but newer DTRMs require evolved capability to transmit and receive digital data at the same time as RF measurements. NI's PXI instruments have the ability to meet measurement requirements of DTRMs, enabling users to build a custom mixed-signal instrument using available VST and HSS modular instruments with power supplies and VNAs to match overall test requirements.

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Image: Sarayut Thaneerat | Dreamstime

CHAPTER 5:

Emerging Cloud Tech Creates Certification and Verification

ULTAN KELLY, Senior Director, *VIAVI*

Where are we in the cloud today when it comes to testing and verifying application solutions and infrastructure?

One of the often-overlooked aspects of our modern society is the layered, multifaceted, and interconnected nature of the technical ecosystem it relies on. The IoT and other cloud-based systems are wireless solutions based on massive amounts of wiring behind the walls and the infrastructure it connects.

These systems, both wired and wireless, are continuously increasing in scope, size, and complexity, challenging those who must design, test, and troubleshoot them. The development of the next generation of solutions based on 6G telecommunications, edge computing, AI, and their related infrastructures is the next great challenge to the electronic design engineering community. The end result is a mixture of cloud environments that must be addressed.

Data centers have become the backbone of modern computing, enabling the storage, processing, and delivery of data everywhere. You can think of hyperscalers as data centers that specialize in delivering massive amounts of computing power and storage capacity to organizations and individuals around the world.

By ensuring seamless scalability with the ability to handle massive workloads without compromising on performance or efficiency, hyperscalers support edge-based cloud environments and enable cloud solution companies that are pure IP. This "fabless" development environment creates additional verification and compliance concerns.

Verification and Compliance in the Cloud

Now the industry is starting to recognize that these open interfaces make for an interoperability nightmare, with various levels of maturity for some of them. For example, the open fronthaul between the radio unit and the baseband unit is now quite mature for single radio deployments, but issues arise when you get into massive MIMO. The industry is beginning to create blueprints for vendors with this cloud technology stack for a particular set of features.

They're taking all possible combinations and permutations in terms of the number of vendors and the number of features that can work together. Every deployment is slightly different and sufficiently different whereby it must be tested to avoid costly combinations. Some are migrating to a continuous integration, development, and test environment.

This is where VIAVI comes into play, as our virtualized and containerized solutions can now run a set of regression tests every time to do a software update. Once that passes, it gives the customer service provider (CSP) the confidence that it can deploy the new version of software in the cloud.

VIAVI made a conscious decision to move away from FPGAs and toward x86 architectures to benefit from the cost savings that it would bring us. It was a general trend that we saw with our more progressive customers.

The company had virtualized a security test solution and moved it into AWS to test that firewall, which you could click and select for extra security 10 years ago, before its acquisition. So, we were familiar with the space, but in a different industry. And we brought that expertise to the wireless customers who had this idea of moving toward the cloud. Now the cloud has gained critical mass and momentum, such that the next round of expansion by operators will see a deployment of control solutions in cloud technologies.

Network Test and Verification

To support a successful transition to a more functional cloud environment, test practices must be developed and refined to ensure the consistent wireless performance demanded by end-users. An ecosystem of collective tools, software, protocols, and practices are required for all wireless cloud deployments to verify the download speeds, latency, and coverage density. Advanced test solutions are playing a vital role in the development, deployment, and operational excellence of emerging wireless networks.

All big changes require commitment, and next-generation cloud-enabled performance is no exception, with complexity and technical challenges to the test arena. Companies like VIAVI have created a fully integrated selection of cloud-enabled test devices and equipment, software automation services, and network test solutions.

Wireless testing has become a critical enabler of cloud potential, and test solutions have quickly adapted to complex use cases and wholesale architectural advances encompassing core, transport, radio access network (RAN), and fiber network elements simultaneously. This has necessitated advanced emulation and verification technology in the test lab that's scalable to full deployment in the field.

For example, 5G fiber networks are being challenged to meet fronthaul and backhaul demands, with the bar set higher for speed, bandwidth, reliability, and synchronization while network function virtualization and edge computing introduce additional visibility obstacles. This convergence of dynamic system elements makes automated, real-time intelligence platforms another important pillar of 5G network performance testing and optimization necessary.

The combination of millimeter-wave (mmWave) utilization, MIMO, and beamforming comprises the infrastructure of 5G, and the added complexity introduced by these innovations can also pose challenges for 5G test networks as well as the overall 5G testing process. MIMO essentially means more antennas, which means a higher burden for 5G testers, as measurement connectors for each antenna will no longer be feasible based on the architecture and density.

Using mmWave and beamforming at these high frequencies presents additional obstacles, since they are more susceptible to propagation loss from environmental conditions, making over-the-air (OTA) testing potentially less consistent and more complex. Since conducted-mode testing can't be performed without discrete connection points, OTA will be required more frequently to avoid limited results.

Channel emulation is also more complex with 5G, as the number of RF channels exponentially increases versus the linear expansion that occurred with 3G and 4G releases. 5G test equipment must involve creative solutions that minimize chamber testing and other expensive test elements, without compromising test coverage and accuracy.

AI in Cloud Solution Testing

AI is becoming more useful in the creation of test solutions for the cloud. One of the products offered by VIAVI is called RIC test, an AI-assisted RAN intelligent controller designed to optimize RAN resources, reduce signaling, and improve capacity (**see figure**). We have a RAN scenario generator product for datasets to enable AI-based algorithms to optimize the network. So, we came up with hundreds of scenarios to generate tens of thousands of datasets to train ML-based models.

The reality is it will take a while for those interfaces to deploy on the network, and the algorithms themselves don't distinguish between real-time, near real-time, or non-real-time because the algorithms will run off the datasets that they have available. What we see now is that the industry has taken a more pragmatic approach, with access to the

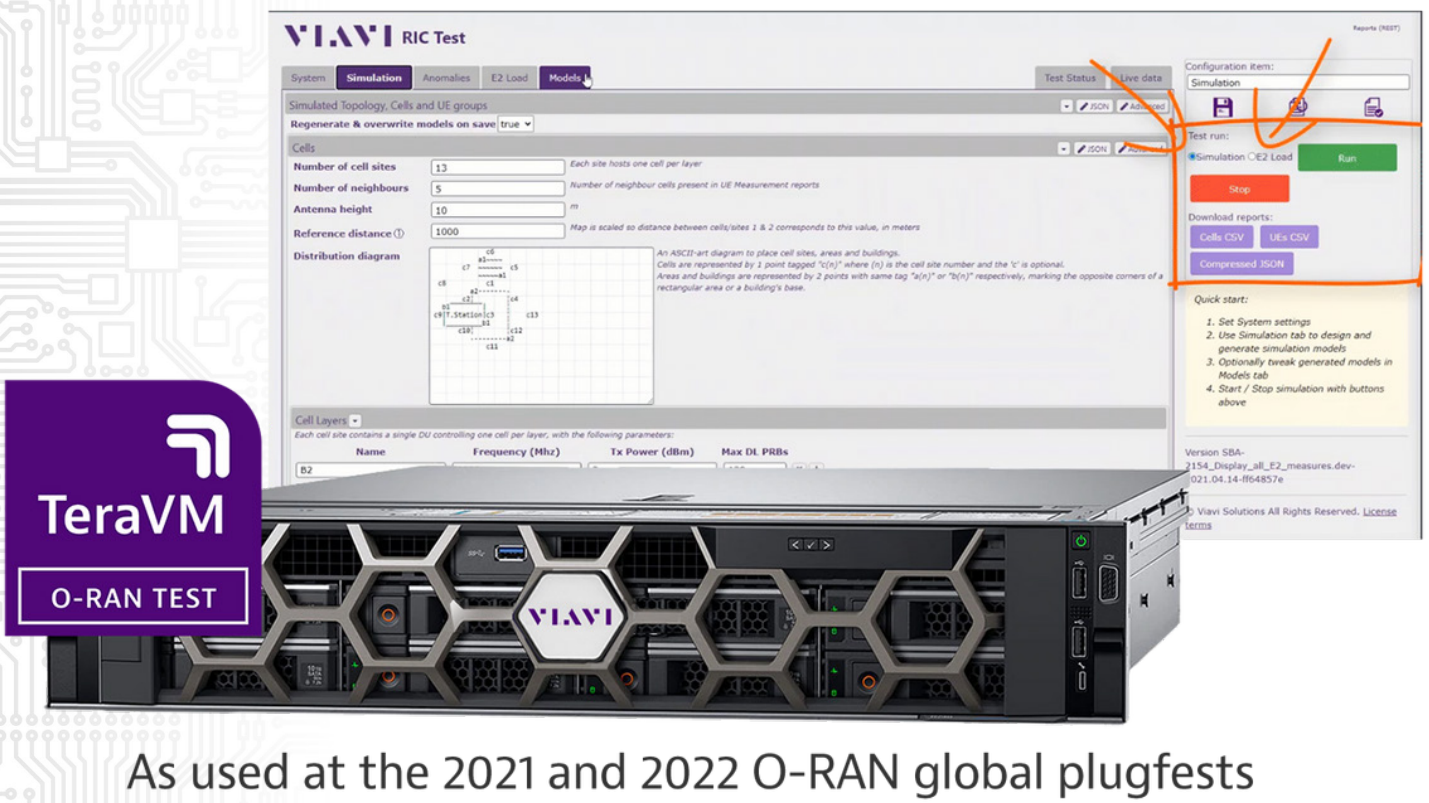

Figure 1: The RIC test solution is an AI-assisted RAN intelligent controller designed to optimize radio access network resources.

datasets and management systems. We will take those datasets and apply the machine-learning models to the data we have. In essence, they're going to bypass the RIC until that technology is available on the network.

You will see more AI-based RAN optimization decisions soon. We're helping the operator develop our own AI models that predict the best possible outcome based on the constraints set by the operator.

A good example is power savings—if I want to save power in the evening time, I want to do it at the expense of quality of experience based on my policy. My policy might say okay, I'll sacrifice some operational time to save power. But how much I sacrifice is up to the operator. Then the algorithms will determine what cells should be powered down or what advanced sleep modes should be set on my base stations.

We need to have that tradeoff between experience and power, with our algorithms advising the operators how well their machine-learning models have done. In other words, our AI will predict how well their AI algorithms will perform.

One of the problems with such automation is that operators are nervous about what goes on. For example, initially, algorithms might show good results, but they might diverge over time. They want to have a high level of confidence in these algorithms before deploying them. That's now the major challenge for AI.

We're going from very simple machine-learning algorithms all the way up to full-blown semi-cognizant AI systems. It's a lot to take in and relates to our ability to migrate things to technological solutions that may outpace our ability to absorb it. Operators don't want to relinquish control because they don't trust the various algorithms, which might compete. You may have one or more optimization algorithms running on the network, and you might find that they're fighting each other to make the correct decision.

VIAVI believes that the next generation of networks will be deployed using cloud technology, and there will be a mixture of public and private infrastructures over time driven by financial decisions. Is it more cost beneficial for me to run secondaries of my network on public versus private cloud? We don't know how that will pan out, but there will be some successes with the operators choosing hyperscalers to host their infrastructure. Some will probably keep it in-house, and others will have a mixture.

One great example is an operator using a hyperscaler for a disaster recovery scenario. During normal operation, it runs on their infrastructure. However, when disaster strikes and some of their infrastructure is knocked out, they can then fall back to a public cloud. It seems to have the best of both worlds for some operators.

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