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Saving SWaP in Payload-Borne Phased Arrays with Multibeam Beamformers

LEO constellation systems require electronically steered arrays at both ends of the link, with the payload particularly challenging because it operates in a power-limited environment. Learn how multibeam beamforming ICs can deliver low-power, high levels of functionality and scale with mission requirements.

Most common satellite communications were once based on geostationary (GEO) satellites, when only three satellites were required for global coverage. Then, launch vehicles would typically carry only one of these large satellites (>1000 kg). While such deployments were beneficial for broadcast applications in television and radio, there were limitations.

One limitation is the latency involved in communications imposed by the great distance between the user and the satellite. Typical GEO orbits are near 36,000 km, which has an approximate end-to-end latency of 400 ms, approximately 10X higher than point-to-point fiber-optic connections in the United States.[1] Secondly, while the GEO satellite covers much of the Earth, it can't effectively cover its northern or southern poles. As an example, Inmarsat's Global Xpress GEO satellites cover approximately ±75° off the equator.[2]

To create true global coverage, smaller (<500 kg) low-Earth-orbit (LEO) satellites are now being deployed with inclined orbits to cover both major and rural population areas and polar orbits to cover the poles. These constellations comprise from several hundred to several thousand satellites. All of them require beamforming antennas because they travel around the Earth at 27,000 km/h at orbit altitudes of 600 to 1200 km. As a result, end-to-end latency is reduced to approximately 50 ms. Each launch vehicle now carries many satellites for each deployment, so the size and weight of these LEO satellites are critical.

In addition, because LEO satellites were developed to provide high-speed data to the user, it's critical to implement the proper frequency plan. Traditionally, Ku-band (10.7- to 12.7-GHz downlink/13.75- to 14.5-GHz uplink) had been used. Today, there's a drive to higher frequencies with wider bandwidths that can support higher data rates.

K/Ka-band (17.7- to 21.2-GHz downlink/27.5- to 31.5-GHz uplink) is being actively leveraged and many are investigating the Q/V bands (37.5- to 42.5-GHz downlink/47.2- to 51.4-GHz uplink) as the next step up in frequency.

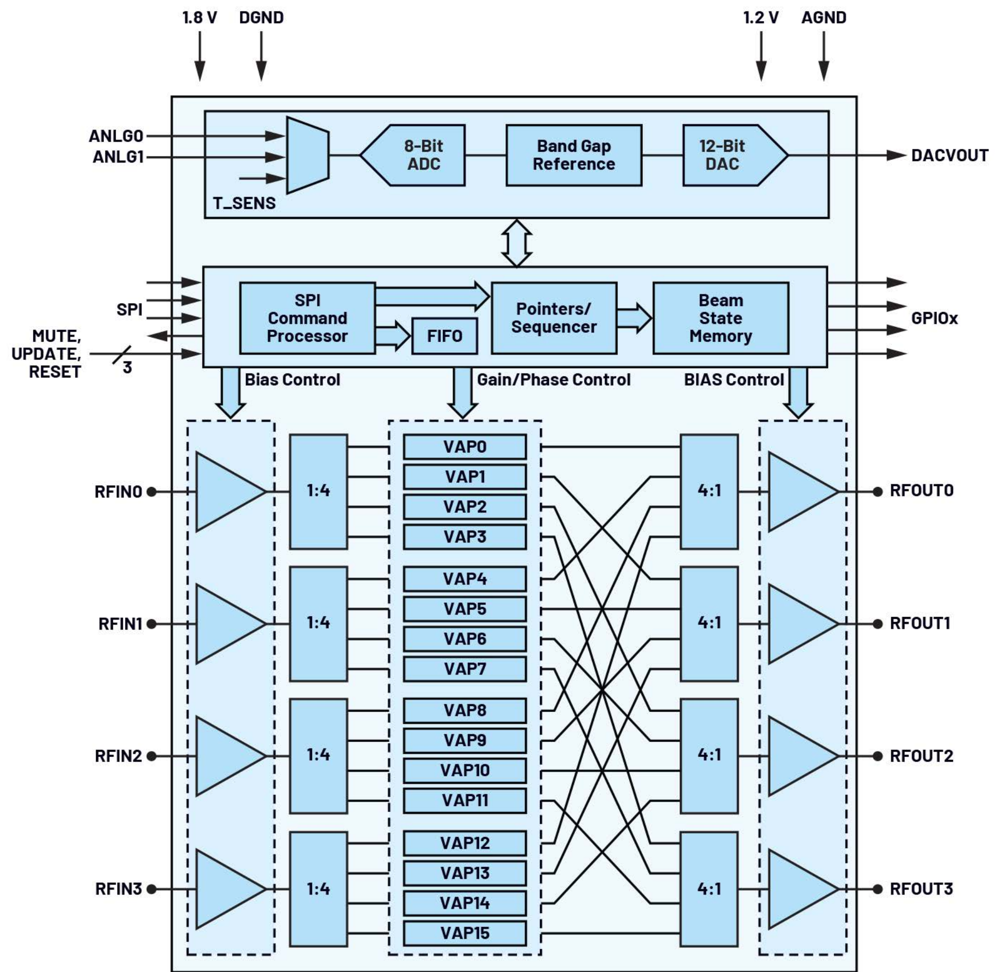
These higher frequencies pose new challenges to the design and realization of a payload phased-array antenna. With increasing frequency, the lattice pitch of the antenna elements decreases, minimizing the available board space.

Traditionally, a discrete approach may have been possible using transmission lines for time delays and phase shifters/digital step attenuators or vector modulators for beamsteering and embedding the Wilkinson splitters/combiners in the printed circuit board (PCB) itself. However, at these higher-frequency bands, the PCB area is a significant challenge, which is driving the need for higher integration for ease of design and manufacturability. In addition, the need for multibeam arrays adds complexity.

Beamforming ICs define electronically steerable phased arrays (ESAs) and serve as the most critical building block. Interwoven in between the beamforming ICs are a power combiner and splitters, which distribute the signals to every beamforming IC. It's the combination of the beamforming IC, power combiner/splitter, and the fabric weaving these two components together in a PCB design that determines the performance of the ESA.

What Comprises a Beamforming IC for ESAs?

To maximize data rate, high-throughput satellites (HTSs) use multiple spot beams to distribute data effectively.



1. Shown is a block diagram of the ADAR3000/ADAR3001 beamforming ICs. These devices are in a 4-beam/4-element configuration that includes 16 VAP channels.

Typical payloads in HTS satellites use multiple beams, which can be steered and hopped to maximize spatial and frequency reuse. Beamsteering is accomplished by changing the phase of the beam as well as the amplitude at each element of the phased-array antenna. To determine the required number of variable amplitude and phase (VAP) devices, multiply the number of beams for the satellite by the number of elements for the antenna—the product is the required number of VAPs.

As an example, for a configuration of 576 elements and 16 beams, the number of VAPs is 9,216 per array. If one considers using a discrete vector modulator as the VAP, which typically is 3 × 3 mm and consumes approximately 0.5 W, will yield a dimension of 0.27 × 0.27 m consuming over 4 kW of DC power. To put this into perspective, a 576-element array at 30 GHz with half-wavelength spacing is 0.113 × 0.113 m. Thus, we require a higher level of integration for higher-frequency payload phased arrays as well as minimal power consumption.

One approach to accomplishing higher integration and lower power consumption comes in the form of Analog Devices' ADAR3000 and ADAR3001 beamforming ICs, which are targeted for K/Ka-band satellite payload applications. These devices are a four-beam/four-element configuration that includes 16 VAP channels. The size of the resultant beamformer is 7 × 12.5 mm, which is a fraction of the array size if using a vector modulator approach.

In addition, to drive down power consumption, the VAP channels use passive structures. In the case of the ADAR3000/ADAR3001, the VAP is constructed of a digital step attenuator (DSA) and digital time-delay unit. This design creates a four-beam/16-channel beamformer that draws less than 200 mW DC *(Fig. 1)*.

These devices, which are designed on a semiconductor process that supports space missions, can be used for LEO/MEO/GEO applications. The beamformers have passed radiation levels of 100 krad of total ionizing dose (TID) and 80 MeV single-event effects (SEE).

Scalability is Critical for Payload Phased Arrays

Not all payload antennas are solely four-beam designs. Higher beam count is required based on the constellation and mission. Beam count is often in multiples of four, so being able to scale a solution from four beams to eight, 16, or 32 beams is critical. ADI's beamformers can be scaled to address higher beam count as well as varying element count. *Figure 2* shows an example of a 16-beam/16-element array.

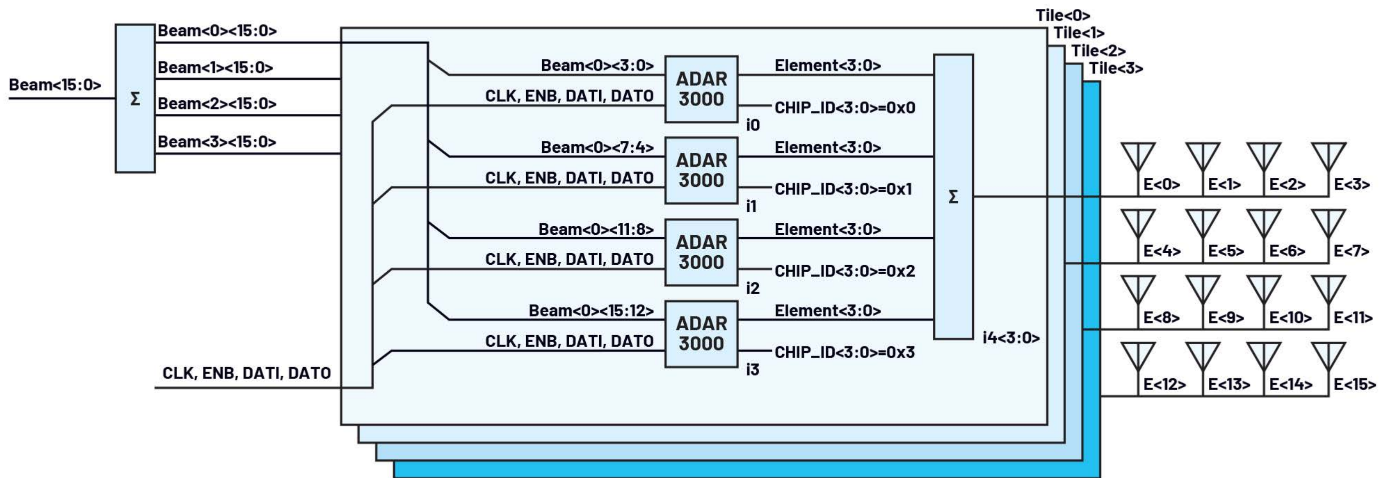
The array in *Figure 2* leverages a blade construction in which each blade consists of four-beam beamforming ICs. For this example, we will look at the transmit antenna, but one can reverse this to support the receive antenna using the appropriate receive beamforming IC.

Because each blade supports four elements, it takes four blades to support 16 elements. And, since each beam needs to be present at each blade, each beam must be split four ways and then routed to each blade. Beams 0 to 3 then drive one of the beamforming ICs, beams 4 to 7 drive the second, beams 8 to 11 drive the third, and beams 12 to 15 drive the fourth beamforming IC.

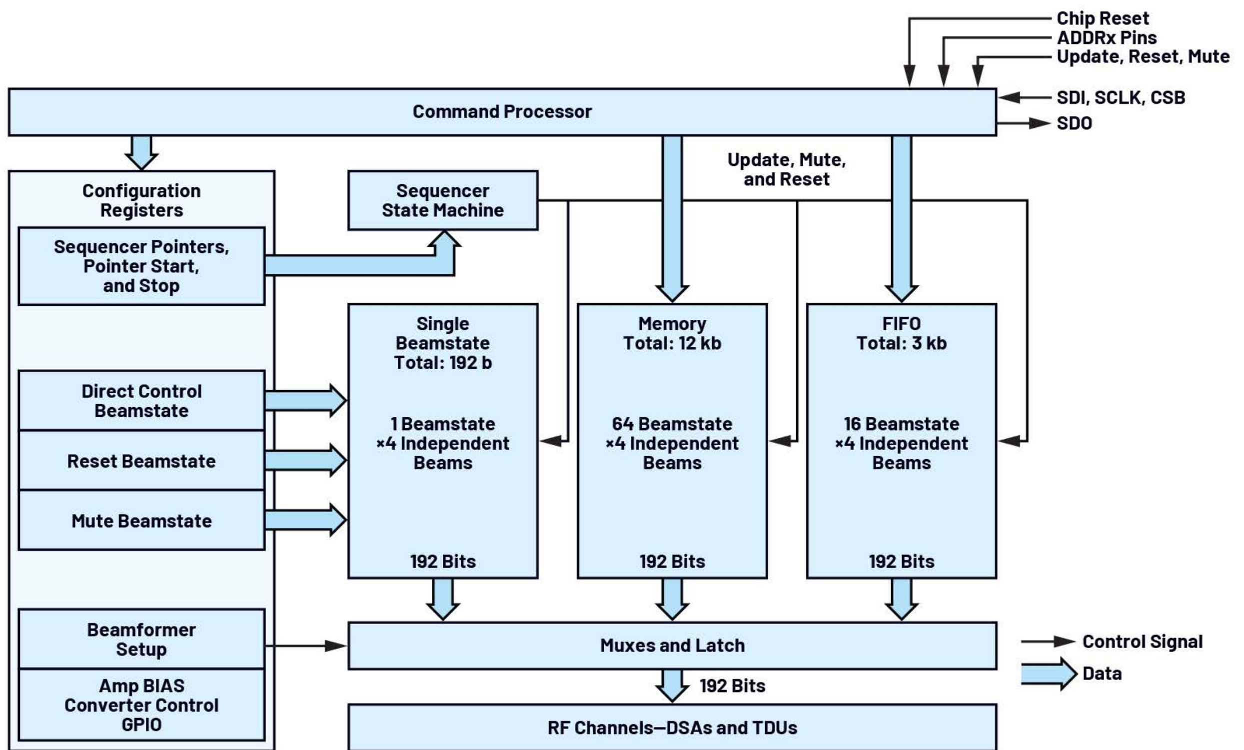
The output of each beamforming IC represents elements

0 to 3 on the array, with each beamformer weighting each beam appropriately for the given position of the element in the array. Because each ADAR3000 IC outputs the beams for elements 0 to 3, the outputs then need to be combined to ensure all 16 beams are present at each element. The same is true for elements 1, 2, and 3. Before driving the elements, the designer should select the appropriate power amplifier (PA) to support the antenna's EIRP and tapering requirements.

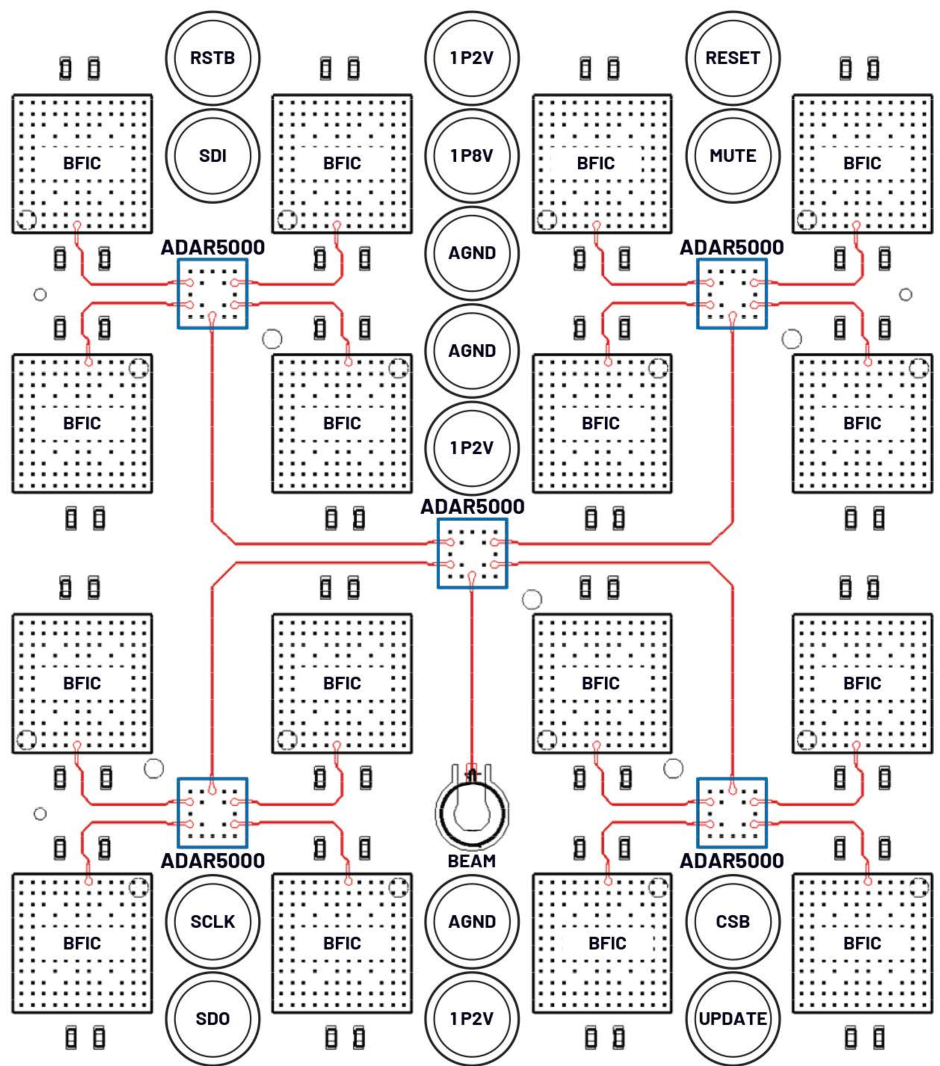
This construction can scale to support more or fewer beams and elements. Increasing the number of tiles will easily support more elements. Adding or reducing the number of beamforming ICs enables the designer to adjust to the number of beams required.



2. The ADAR3000/ADAR 3001 beamforming ICs are scalable to accommodate higher beam counts. This example represents a transmit antenna. Note that the PA and filter aren't shown at the element.



3. Within the ADAR3000/ADAR3001 ICs' digital feature set, the RAM and FIFO have sequencer state machines that increment through the beam states that are stored within.



4. Shown is the routing of a Ka-band beamforming IC laid out in conjunction with the ADAR5000 1:4 splitter for applications requiring a two-dimensional planar design.

Digital Control Aids in SWaP Reduction

In addition to size and power, digital control and functionality are important in the effort to minimize size, weight, and power (SWaP) in the payload. Requirements such as beam hopping must be performed easily and quickly. To support beam control as close to the elements as possible, a sophisticated digital section is integrated into the beamformer IC. It's worth noting that each device has four address lines. Thus, a single SPI bus can communicate with up to 16 beamformers, which minimizes the number of SPI lines and simplifies the array design. Each beam is independently controlled and has its own memory.

The random-access and FIFO memories have their sequencer state machines that increment through the beam states stored within *(Fig. 3)*. The RAM can store up to 64 beam states and the FIFO stores up to 16 beam states.

These features help support beam hopping and raster scanning of the antenna. When using the RAM with the sequencer, one may program up to 64 beam states per beam. Using the sequencer, the beam states can then be loaded in any prescribed sequence. Similarly, when using the FIFO memory, once the beam states are loaded, the beam states can then be loaded in FIFO order.

Note that beam updates are very fast with internal memory. Single VAP response time is < 10 ns. Update-to-update minimum timing is < 50 ns.

Wilkinson Combiner/Splitter Considerations

As previously mentioned, the beamformer IC's design and higher levels of integration within a package offer substantial SWaP advantages. Likewise, the design decision of the power combiner/splitter interlaced between the beamformer ICs needs to be optimized for SWaP tradeoffs. Because the power combiner/splitters face the same design challenges of minimal PCB area due to tight lattice spacing constraints, small size and optimized PCB routing are key for system performance and signal integrity.

First and foremost, the power combiner/splitter for phased arrays is passive. Thermal management for an active phased array is a difficult engineering challenge given the very small size and form factor as well as the high power-handling capabilities. For this reason, the combiner/splitter is passive so as not to further burden the thermal requirements of the phased array.

Important performance characteristics to consider for combiners/splitters are frequency bandwidth coverage, port matching, isolation, minimal parasitic losses, and power handling. Achieving matched ports maintains symmetry where the input power splits evenly across all output ports and the phase difference between the output ports is kept to a minimum. Furthermore, the input and output ports maintain a well-defined characteristic impedance.

The most common power combiner/splitter architecture used in phased-array systems is the Wilkinson design. When all of the ports are well matched, the Wilkinson divider offers the benefits of minimal loss, achieves high

isolation between output ports, and is reciprocal.

Wilkinson designs are commonly implemented directly on the PCB with microstrip and/or stripline. Alternatively, for improved SWaP benefits, monolithic silicon-based Wilkinson designs like the [ADAR5000] and [ADAR5001] prove quite advantageous in conserving PCB area, ease of routing, and improved signal integrity.

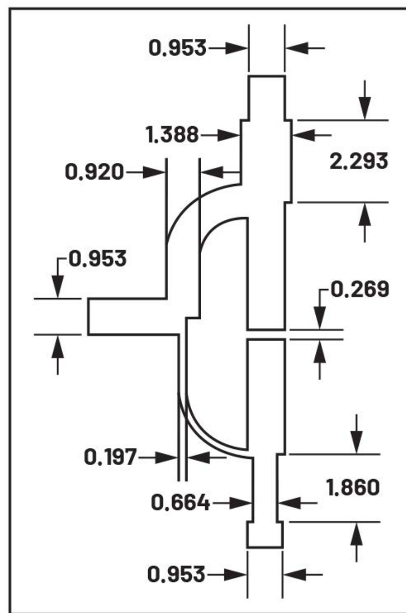
The ADAR5000 RF splitter/combiner is a 1-to-4 Wilkinson power splitter that's designed for space-sensitive microwave signal distribution applications. Excess insertion loss ranges from −1.5 to −2.5 dB from 17 to 32 GHz. The four outputs are matched in both phase and amplitude, suiting this device for signal-distribution applications requiring low time skew between channels. It can also be used as a combiner.

The IC, housed in a 2.5- × 2.5- × 0.5-mm WLCSP, is built for planar, phased-array antenna systems that require a tight pitch between elements. Similarly, the ADAR5001 RF splitter/combiner is a 1-to-2 Wilkinson power splitter in a 1.5- × 1.5- × 0.5-mm WLCSP package.

The ADAR5000/ADAR5001 devices offer substantial PCB area and cost savings over traditional Wilkinson power-divider implementations utilizing a microstrip design on PCB. This is especially true at Ka-band frequencies where the lattice spacing for a phased-array design must be less than 5 mm at 31 GHz to prevent grating lobes. This lattice pitch must be shared between the beamforming IC and the combiner/splitters within an optimized layout structure.

For example, for airborne satcom terminals at Ka-band where the form factor of the complete phased-array system is planar or two-dimensional, the patch antennas reside on one side of the PCB and the beamforming IC and Wilkinson power dividers share the opposite side of the same PCB.

Figure 4 shows the routing of a Ka-band beamforming IC laid out in conjunction with the ADAR5000 1:4 splitter for applications requiring a two-dimensional planar design. The layout is optimized and efficient—the high-frequency traces are localized to the surface layer and the traces are direct, matched, and the shortest path from the device to the beamforming IC. Isolating the high-frequency traces to the surface layer of the PCB allows for more controlled impedances of the traces and minimizes parasitic losses.

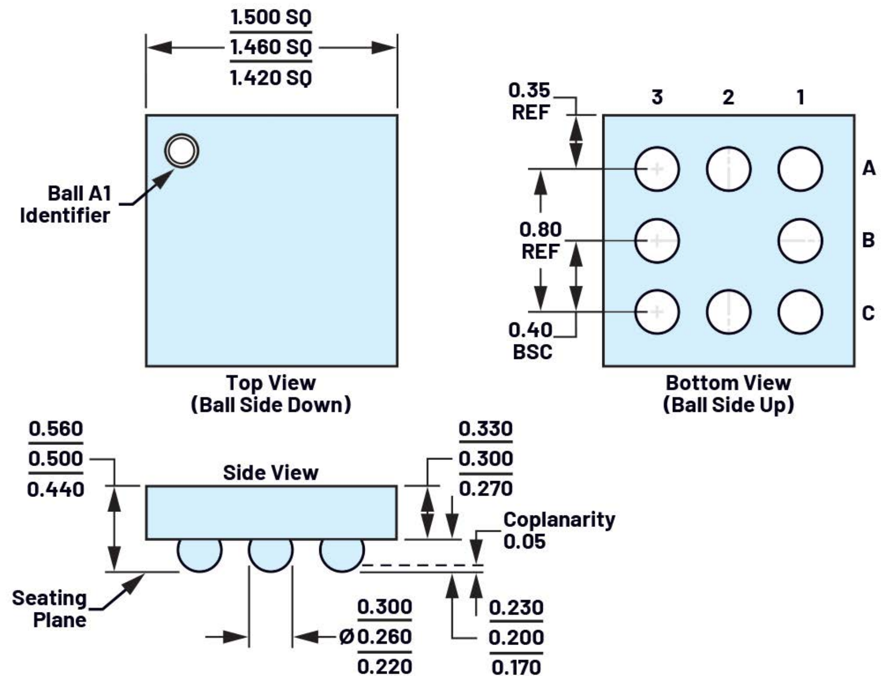


5. This image depicts the layout of a 1:2 microstrip, modified Wilkinson power divider on a Rogers substrate at K- and Ka-band frequencies.

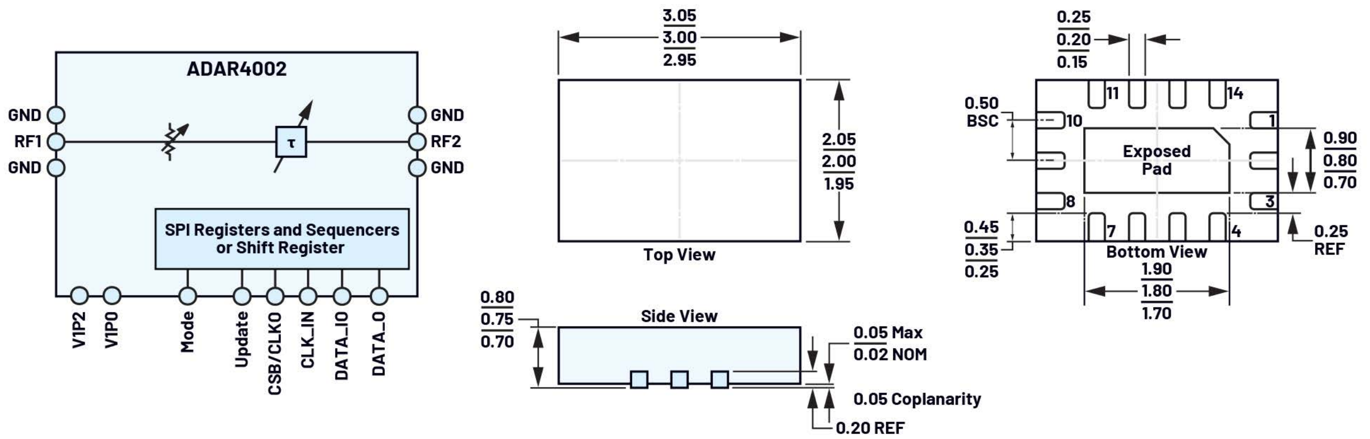
The ADAR5000/ADAR5001 replace the traditional microstrip on PCB Wilkinson power divider designs. A microstrip design at Ka-band requires substantially more PCB area. *Figure 5* illustrates the layout of a 1:2 microstrip, modified Wilkinson power divider on a Rogers substrate at K- and Ka-band frequencies.[3]

Figure 6 shows the required footprint for the ADAR5001, which is substantially smaller in PCB area than the microstrip design. The footprint of the 1-to-2 Wilkinson power divider is in a 1.5- × 1.5-mm package, while the 1-to-4 divider comes in a 2.5- × 2.5-mm package. Only the form factor fits within the lattice spacing for Ka-band frequencies up to 31 GHz.

Moreover, the performance of the Wilkinson power-



6. Here's the required footprint for the ADAR5001 1:2 Wilkinson power divider, which is substantially smaller in PCB area than the microstrip design.



7. Shown is the ADAR4002 block diagram and package outline for a 14-lead, lead-frame, chip-scale package (LFCSP) measuring 3 × 2 mm with a 0.75-mm package height.

divider design depends heavily on the matching of the ports. The matching of the ports can only be as good as the tolerances of the manufacturing process of the PCB. Silicon tolerances are tighter and allow for smaller geometries.

Time Delays Provide Mismatch Compensation

To further improve and facilitate the system design of a phased array utilizing a corporate feed network, the ADAR4002 time-delay unit provides extended time-delay and amplitude control in a single-channel, low-power, and miniaturized package. Given these features, it's a suitable component to distribute in a design to add slight adjustments in delay due to mismatches. It also serves to add more delay compensation as needed for a true time-delay phased array where the delay is inefficient to cover the bandwidth.

The ADAR4002 is a low-power broadband, bidirectional, single-channel, true time-delay unit (TDU) and a DSA. The frequency coverage of the device extends from 500 MHz to 19 GHz with 50-Ω input impedance at both RF ports. The TDU has two programmable maximum time delays, each with a 7-bit control. Range 0 has a maximum delay of 508 ps with a resolution of 4 ps. For low-frequency operation, Range 0 would be selected because more time delay is available for a full 360-degree phase coverage.

Range 1 has a maximum delay of 254 ps and a resolution of 2 ps. This range has less insertion loss compared to Range 0 and is more suited for high-frequency operation due to a narrow delay range with finer controls of the step size. The DSA has a 6-bit resolution with an attenuation range of 0 dB to 31.5 dB and a step size of 0.5 dB *(Fig. 7)*.

Regarding the SWaP advantages of the ADAR4002, the passive nature of the device's core building blocks results in substantial power savings. The TDU and DSA are passive while the digital control is the only block that consumes power. With this said, this device is designed to provide flexible digital control through either a serial port interface (SPI) or a shift register. The

Table 1. Propagation Delay for a Few PCB Materials[4]

Material	Er	Er_{eff}	V Microstrip	V Stripline	t_{pd} Microstrip	T_{pd} Stripline
Vacuum or Air	1	1	11.8 in/ns	11.8 in/ns	85 ps/in	
Isola 370HR	4.0	2.92	6.90 in/ns	5.9 in/ns	145 ps/in	170 ps/in
Isola I-Speed	3.64	2.69	7.20 in/ns	6.18 in/ns	139 ps/in	162 ps/in
Isola I-Meta	3.45	2.57	7.36 in/ns	6.35 in/ns	136 ps/in	158 ps/in
Isola Astra MT77 or Tachyon 100G or Rogers 3003	3.0	2.28	7.8 in/ns	6.8 in/ns	128 ps/in	147 ps/in
Rogers 4000 Series	3.55 — 3.66	2.63 — 2.7	~7.20 in/ns	~6.20 in/ns	~139 ps/in	~161 ps/in

shift register allows for daisy chaining of multiple chips.

The IC also contains register memory for 32 TDU and DSA states. The memory combined with on-chip sequencers allows for fast bidirectional memory advancement via the Update pin. These digital features prove advantageous for ease of use and fast beam hopping. The ADAR4002 consumes a total of 1 mW with 1.2- and 1.0-V dual supplies.

With its broad time-delay range, in a 2- × 3-mm LFCSP package, the ADAR4002 has a number of potential use cases. It can be placed strategically in a design to compensate for PCB length or delay tuning. Because of the difficulty in matching the lengths of all PCB signal lines in very large phased arrays, it may be necessary to introduce delay tuning. The goal is to set the lengths of signal traces in a matched group of nets to the same length value. This ensures all signals arrive within some constrained timing mismatch.

The most common means of achieving signal-trace synchronization is to increase delays in the shorter traces by adding some trace meandering such as trombone, sawtooth, or accordion. Trace meandering comes at the expense of PCB area and design time because a unique trace is required for a specific time delay.

To put this into perspective, for a high-frequency board material such as Isola Astra MT77 or Rogers 3003, where the dielectric constant is 3.0, approximately 3.5 inches of stripline or 4 inches of microstrip is required to achieve 508 ps of delay. *Table 1* shows the propagation delay for a few PCB materials as collected by the Sierra Circuits Team.[4] The PCB area required is quite substantial compared to the small 2- × 3-mm package of the ADAR4002, which offers a range of delays in a single footprint.

Traditional discrete approaches to the design of phased arrays for satellite payloads aren't optimized for size, weight, or power. GEO satellites are large satellites where a single satellite resides on a launch vehicle. By contrast, today's LEO constellations require deploying many satellites on a single launch vehicle, which limits their size and weight.

In addition, the demand for higher data throughput is pushing satellite communication frequencies from Ku-band to K/Ka-band and higher, requiring even smaller antenna arrays. Advances in silicon-based ICs have added higher levels of integration, functionality, and lower DC power consumption, which make for smaller, thinner, and lighter antenna apertures to support Ku-band frequencies and higher to address the SWaP challenges of today's satellites.

Qui Luu received her BSEE from Worcester Polytechnic Institute in 2000, and an MSEE degree from Northeastern University in 2005. Since 2000, she has been with Analog Devices Inc., where she is currently a system engineer/IC architect in the Aerospace and Defense Organization located in Chelmsford, Mass. Her focus area as of late has been on beamforming ICs and system development from the antenna to bits for electronically steerable phased arrays.

John Wise received his BSEE from the Illinois Institute of Technology. Before retiring, he was the product line manager for beamforming ICs and SiPs in Analog Devices' Aerospace and Defense organization. Prior to joining ADI, Mr. Wise held positions at Hewlett-Packard (now Keysight) and Hittite Microwave. He has over 30 years of experience in the design, development, and production of microwave and fiber-optic test equipment, components, modules, and custom assemblies and ICs for commercial, military, and hi-rel applications.

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