

# Clock Spur Suppression in Phased-Array RF Subsystems

RF absorption and PLL phase calibration help phased-array subsystems reduce clock spurs while preserving spectral purity and channel coherency.

In high-performance RF systems, maintaining exceptional signal purity is essential to ensure accurate signal representation and optimal dynamic range. Clock spurs — unwanted tones resulting from clock leakage or coupling into sensitive analog signal paths — pose a significant threat to system performance. These spurious components can elevate the noise floor, reduce spurious-free dynamic range (SFDR), and compromise overall signal integrity, particularly in [direct-RF-sampling architectures](#) where clock and data domains are tightly integrated.

Within the Quad-Apollo MxFE platform, detailed signal-integrity analysis revealed that clock spurs originated from the [ADF4382](#) ICs, with radiative coupling mechanisms introducing periodic interference into the DAC output traces. Such coupling not only produced coherent spectral artifacts, but it also affected system-level linearity and [multichannel synchronization](#).

To address these issues, a comprehensive mitigation methodology was implemented, combining physical and digital countermeasures. On the hardware side, enhanced electromagnetic shielding, improved ground isolation, and strategic PCB layout optimization were employed to minimize radiative and conductive coupling between high frequency clock networks and analog signal paths.

Complementing those measures, a precise digital phase-calibration algorithm was introduced to decorrelate residual spurious components, effectively suppressing any remaining coherent clock feedthrough.

This hybrid approach — integrating robust hardware shielding with intelligent digital correction — significantly reduced clock spur levels, restoring SFDR performance and ensuring stable, deterministic operation across all [JESD204C data links](#). The resulting improvements underscore the importance of system-level mitigation

strategies in achieving ultra-clean spectral performance in next-generation high-speed RF platforms.

## High-Level Procedure

The spur decorrelation methodology in the Quad-Apollo MxFE platform integrates both physical mitigation and algorithmic calibration techniques to systematically eliminate clock-induced spectral artifacts. This structured process ensures that all data converters operate coherently while minimizing interference from coupled clock energy. The approach can be broken down into the following key stages:

1. **Spur identification:** The process begins by isolating the specific clock spur or harmonic that most significantly impacts overall system performance. Spectral-analysis tools are used to measure spur levels at various operating conditions, identifying the dominant contributor to SFDR degradation.

2. **Phase rotation:** Once the critical spur is identified, controlled phase adjustments are applied to the sample clocks of selected phase-locked-loop (PLL) ICs, while one device remains fixed as the timing reference. This controlled phase rotation enables the characterization of spur behavior as a function of relative clock phase.

3. **Spur monitoring:** As phase offsets are introduced, the system continuously monitors the resulting spur magnitude using spectral measurements or FFT-based evaluation. By mapping spur amplitude against clock phase, the configuration yielding the lowest spur power can be precisely identified.

4. **Phase application:** After determining the optimal clock phase combination, the corresponding phase settings are permanently applied to the targeted PLL ICs. This ensures that the selected phase offset aligns all converters in

a configuration that minimizes coherent spur reinforcement.

5. **Iterative calibration:** The same process is repeated for additional PLL devices, always referencing the same fixed clock source. This iterative refinement gradually decorrelates clock spurs across all participating ICs, achieving a system-wide reduction in spur amplitude.

6. **System calibration:** Following the spur decorrelation phase, fine-tuning is performed across the transmit (Tx) and receive (Rx) signal paths within the RF front end. This stage compensates for any residual phase mismatches introduced by analog propagation delays, ensuring consistent timing across all RF channels.

7. **Digital signal processing (DSP) coherency:** Finally, the Apollo MxFE system's hardened DSP numerically controlled oscillator (NCO) phase shifters are used to maintain coherent digital phase alignment across all data paths. This ensures that the system preserves phase coherency for [beamforming](#) and other multichannel DSP functions, even after the physical and calibration-based spur suppression stages.

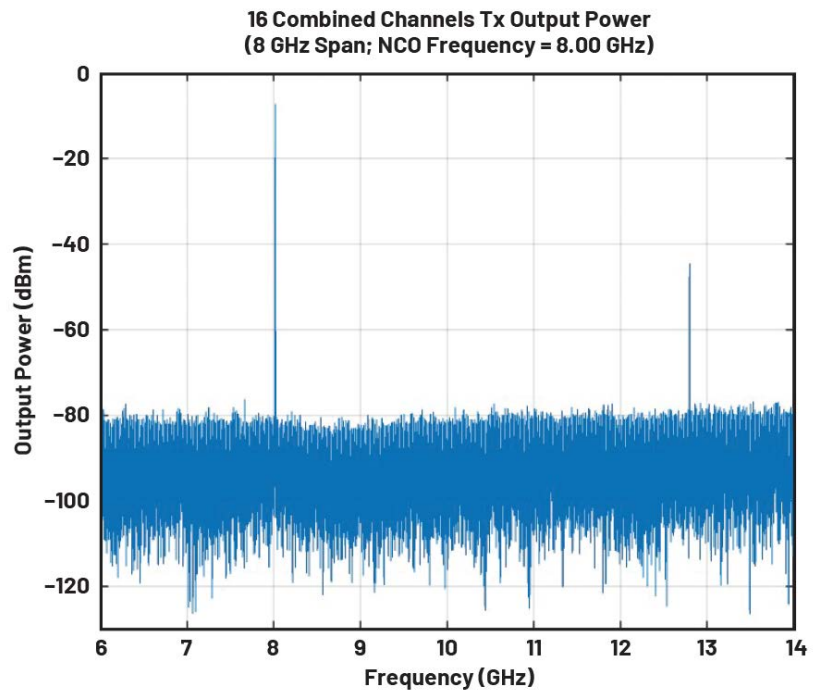
By combining precise clock-phase manipulation, iterative calibration, and digital coherency control, the Quad-Apollo MxFE platform achieves substantial spur suppression while maintaining full synchronization and phase stability across all channels. This hybrid approach exemplifies how coordinated analog and digital design practices can jointly enhance spectral purity in complex RF systems.

### Initial Characterization

Initial system characterization revealed that the SFDR was constrained by unwanted clock leakage manifesting within the DAC output spectrum (*Fig. 1*). Detailed spectral measurements indicated the presence of discrete spurious tones at harmonic offsets corresponding to the system clock frequency, suggesting a coherent coupling mechanism rather than random noise interference.

Further investigation traced the root cause to radiative and conductive coupling from the PLL ICs, which generated strong clock harmonics that inadvertently coupled into neighboring DAC output traces. The physical proximity of high-frequency digital clock lines to sensitive analog signal paths created an environment conducive to electromagnetic radiation and trace-to-trace crosstalk.

These coupling effects effectively injected clock-related energy into the DAC outputs, resulting in repeatable,



1. Transmit characterization plot showing combined channel performance across 6 to 14 GHz. (Credit: Analog Devices)

phase-coherent spurs that degraded overall SFDR and compromised signal linearity.

This observation established clock leakage as the dominant limiting factor in the system's spectral purity and guided the development of a targeted mitigation strategy. It involved combining hardware shielding, improved layout practices, and algorithmic phase decorrelation to suppress these artifacts at their source.

### RF Absorption Wall Installation

To address the radiative coupling mechanism responsible for clock leakage into DAC outputs, RF absorption material was strategically installed around the heatsinks of the PLL ICs. This material functions as a lossy electromagnetic barrier, dissipating radiated clock energy as heat before it can couple into adjacent sensitive analog traces.

The goal of this modification was to suppress near-field radiation from high-speed clock domains without altering the electrical characteristics of nearby transmission lines or disrupting thermal management.

#### Initial Results

Following installation of the RF absorber material — without any additional calibration or phase adjustment — the system demonstrated a substantial improvement in spectral purity. Measured spur levels dropped by approximately 15 dB, decreasing from  $-45$  dBm to  $-60$  dBm. This immediate improvement confirmed that a significant

portion of the spurious energy was radiatively coupled, and that absorption material alone could effectively attenuate these emissions.

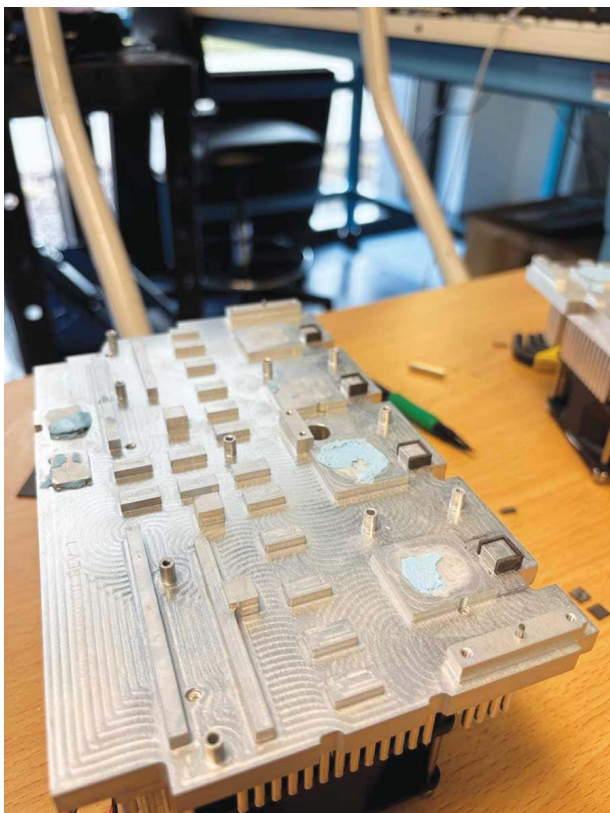
#### Further Calibration

Building on the hardware-based improvement, an additional digital calibration stage was applied. After the absorber material was installed (on a Quad-Apollo MxFE board without heatsinks), the PLL phase-calibration script was executed to optimize clock phase relationships across devices.

This algorithmic phase rotation yielded a further 20-dB reduction in spur amplitude, achieving a total clock spur suppression of approximately 30 dB and reaching a final spur level near -75 dBm. The combined use of passive absorption and active phase decorrelation proved highly effective in minimizing coherent clock feedthrough.

#### Design Considerations

In implementing the absorptive shielding, careful attention was paid to mechanical and electrical layout constraints. Absorption walls (Fig. 2) were positioned to provide effective isolation around the PLL ICs while ensuring that the primary sample clock distribution paths remained unobstructed. The absorber placement also preserved controlled impedance along critical PCB transmission lines



2. RF absorption material installation on heatsink around PLL touch-downs. (Credit: Analog Devices)

(Fig. 3), avoiding any adverse effects on signal integrity or clock distribution performance.

This combination of targeted RF absorption and precise digital calibration established a robust methodology for reducing radiative coupling and enhancing SFDR performance in dense, high-speed mixed-signal systems such as the Quad-Apollo MxFE platform.

#### System Calibration with Absorber

Before phase rotation calibration, a system-level calibration was performed with absorbers installed. This step aimed to assess the baseline spur levels and output power to assess if the absorber application affects the system calibration in any way. Results of this baselining can be seen in (Fig. 4) and (Fig. 5).

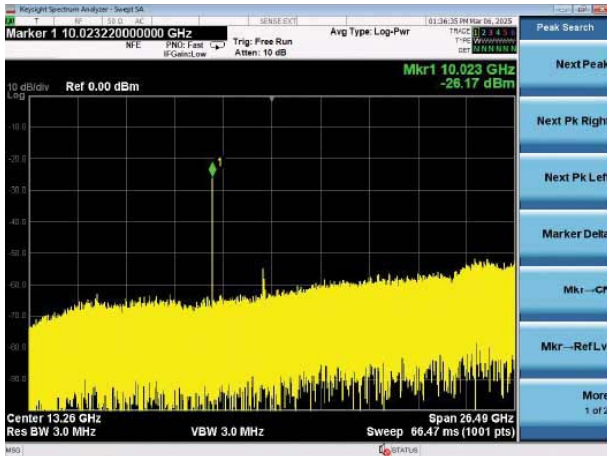
#### PLL Phase Rotation Calibration

Phase rotation calibration was performed in three steps, each targeting a different PLL IC:

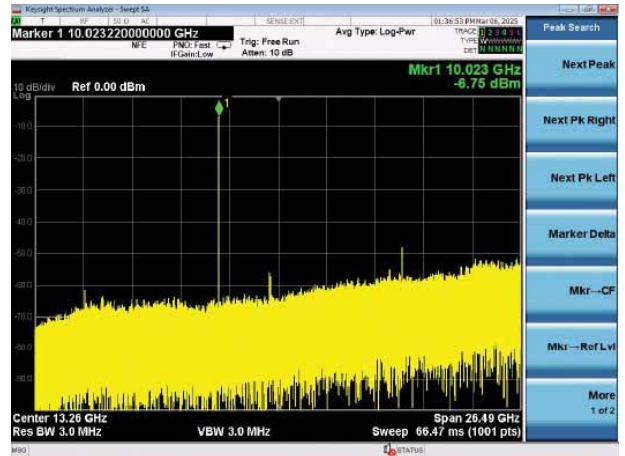
- **Step 1:** Rotate the first ADF4382 (channels 1 and 5 active) in 5° increments from 0° to 360°, then refine in 1° steps to find the null.
- **Step 2:** Add Channel 9 and rotate the second ADF4382 similarly relative to the already nulled first PLL pair.



3. RF absorption wall close-up. (Credit: Analog Devices)



4. Single-channel output (-26.17 dBm). (Credit: Analog Devices)



5. Combined channel output post-calibration (with absorber applied, clock spur power ~-55 dBm). (Credit: Analog Devices)

- **Step 3:** Add Channel 13 and repeat the rotation of the third ADF4382 and null-finding relative to the first and second PLL pairs. See *Figure 6* for the null finding result at this step.

### Performance Metrics

Following the PLL phase rotation calibration and RF absorption wall installation, the Quad-Apollo MxFE platform demonstrated significant improvements in both output power and spectral purity. These metrics were evaluated across a range of operating frequencies to assess the robustness of the spur mitigation strategy.

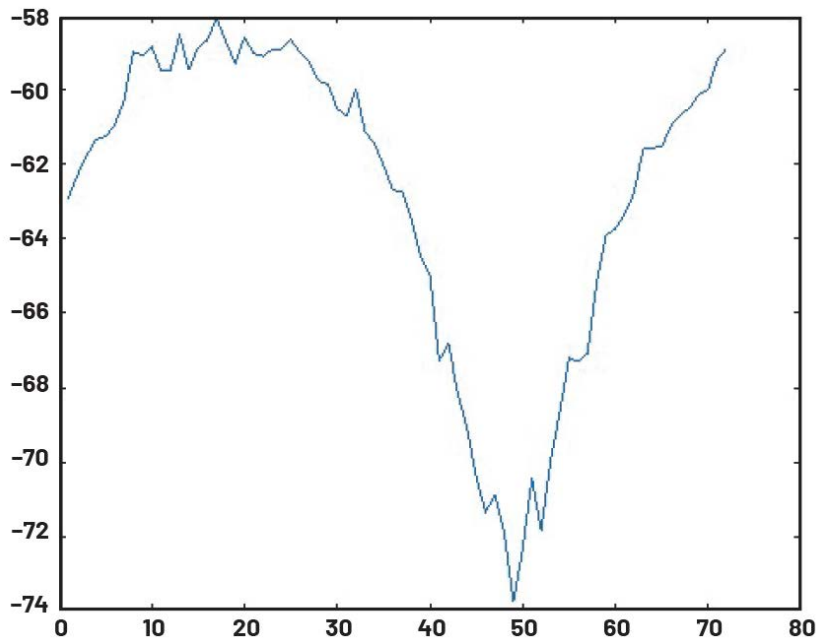
The calibrated system showed a consistent increase in transmit output power across all active channels. This improvement is attributed to reduced interference from clock spurs, which previously limited the effective dynamic range of the DAC outputs. The enhanced power levels indicate that the signal path is now less contaminated by unwanted spectral components, allowing for more efficient signal transmission.

*Figures 7 and 8* show how we preserve the transmit output power of the system while still obtaining a drastic improvement in SFDR after running the calibration process.

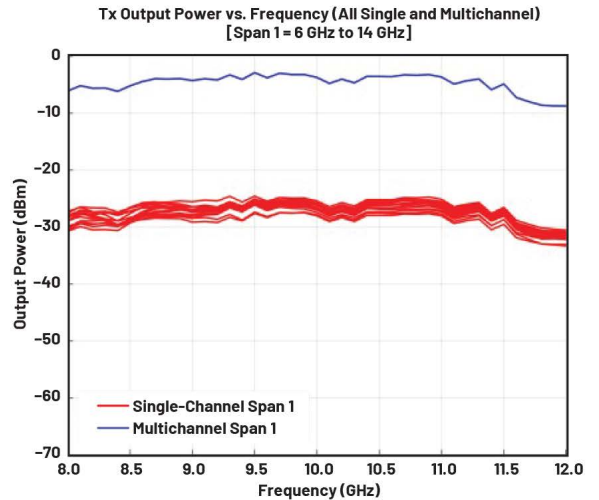
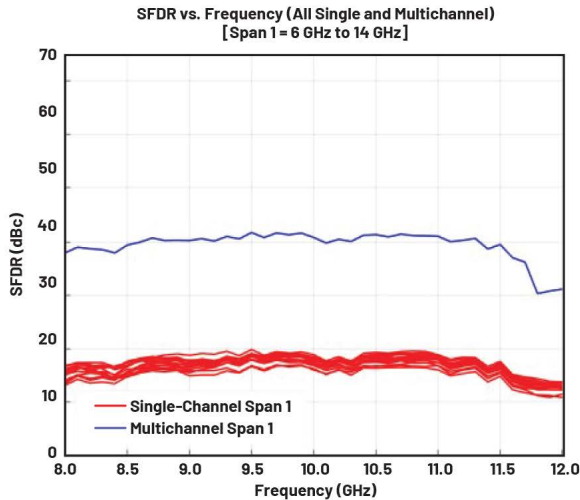
SFDR is a critical metric in RF systems, representing the ratio between the fundamental signal and the strongest spur within the bandwidth of interest. Post-calibration measurements revealed a substantial increase in SFDR, confirming

the effectiveness of the decorrelation efforts. The system now operates with a cleaner spectral profile, which is essential for applications requiring high linearity and low distortion.

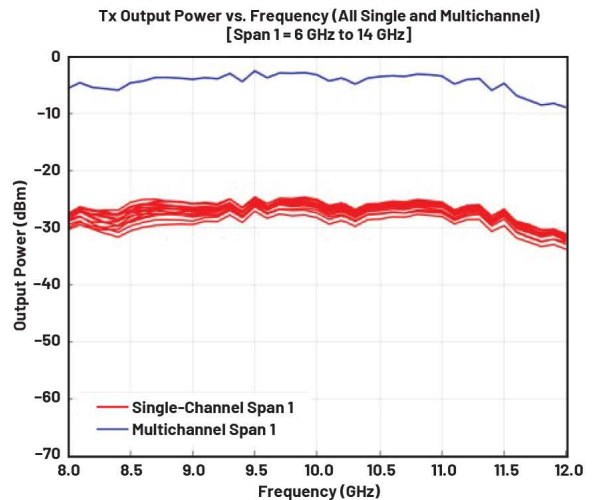
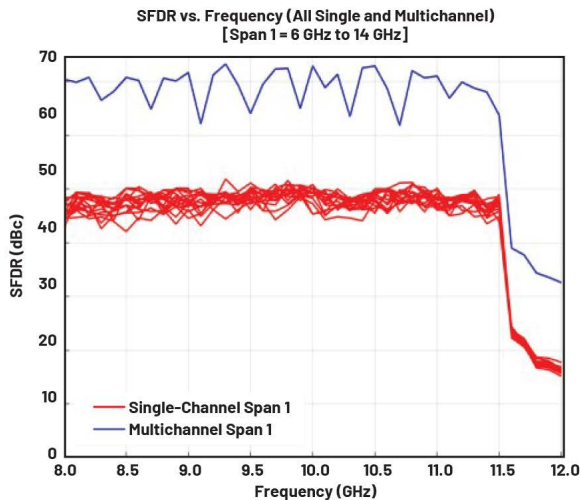
The improvements in output power and SFDR were consistent across the tested frequency range, indicating that the calibration and shielding techniques aren't frequency-dependent. This suggests that the methodology can be generalized to other configurations or future revisions of the Quad-Apollo MxFE platform.



6. Null-finding calibration result (monitoring clock spur magnitude at Step 3). (Credit: Analog Devices)



7. Transmit SFDR and output power vs. frequency (before phase rotation calibration). (Credit: Analog Devices)



8. Transmit SFDR and output power vs. frequency (after phase rotation calibration). (Credit: Analog Devices)

### Conclusion

The Quad-Apollo MxFE clock spur decorrelation initiative successfully demonstrated a multifaceted approach to mitigating clock-induced interference in high-speed RF systems. By combining physical shielding using RF absorption materials with precise digital phase calibration of PLL ICs, the team achieved over 45 dB of spur suppression. This not only improved the system's SFDR, but it also enhanced the overall signal integrity and output power.

The calibration process proved to be repeatable and scalable, showing consistent results across multiple channels and frequency ranges. Importantly, the improvements were achieved without compromising JESD link stability, confirming the robustness of the approach in real-world system conditions.

These results validate the effectiveness of combining hardware and software techniques for spur mitigation and open the door for further optimization. Future work may

explore automating the phase rotation process, integrating real-time spur monitoring, and extending the methodology to other platforms or IC configurations.

Ultimately, this work contributes to the broader goal of enabling cleaner, more reliable signal chains in next-generation RF systems.

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